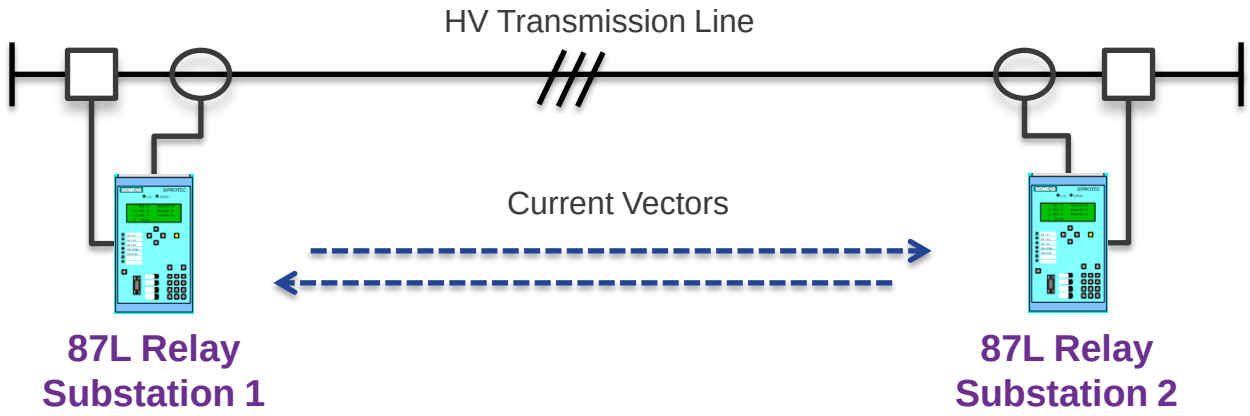
Proving Viability of Line Current Differential over Packet Switched Networks

Silvio Roesler, Siemens Energy

Ruben Lobo, Cisco Systems, Inc.

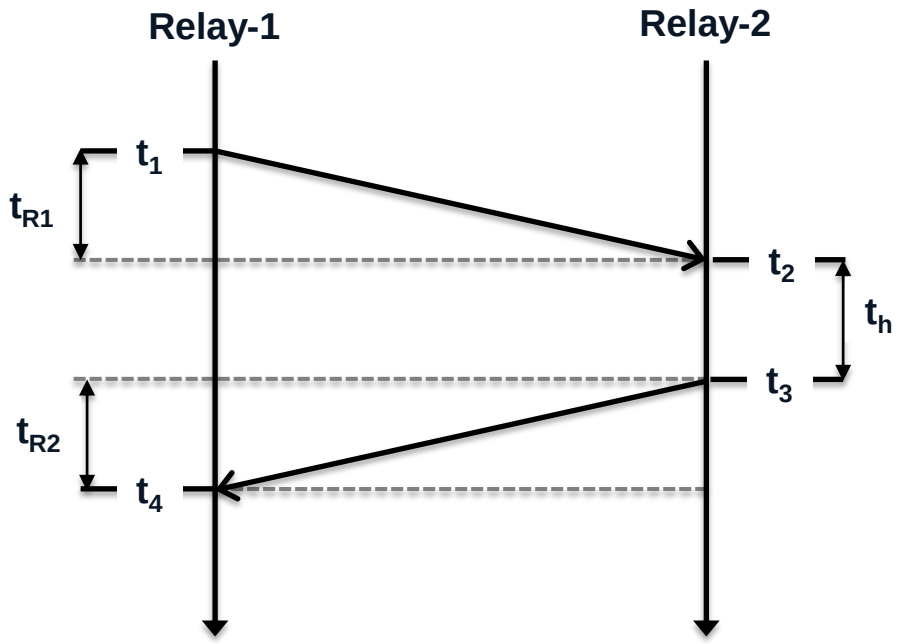
April 2, 2014

Line Current Differential Protection



- Operates on the principle of comparing current samples across the two end of the protected line
- Current samples from the two line ends must be time aligned for comparison
  - Phase angle shift caused due to time synchronization error will produce a fake differential, leading to a false trip
- Two mechanisms can be use to time synchronize the relays
  - GPS based synchronization
  - Channel-based synchronization

Channel-Based Synchronization



$relayClockOffset = t_2 - t_1 - meanPathDelay$

$meanPathDelay = ((t_2 - t_1) + (t_4 - t_3)) / 2$

- Technique used by 87L relays to time-align current samples over communication channel
- No dependency on GPS
- Also known as “Ping-Pong” or “Echo” scheme
- Proprietary vendor specific implementations, but based on the common principal of two-way exchange of time-stamped messages
- Round-trip delay is measured on the assumption that transmit and receive latency between relays is symmetric
- IEEE 1588 PTP is an example of a two-way time transfer protocol that works on this principal

Impact of Latency, Latency Asymmetry, and PDV

Latency

- Influences time to transport current sample to remote end for comparison
- Impacts time for relay to be made aware of a fault differential

Latency Asymmetry

- Applies only to 87L relays dependent on channel-based synchronization
- Skews *relayClockOffset* computation, leading to time synchronization error
- Latency asymmetry would need to be compensated by the relays, resulting in lowered sensitivity of protection
- Drives the requirement of symmetric forward and return paths between 87L relays

Packet Delay Variation (PDV – “Jitter”)

- Applies only to 87L relays dependent on channel-based synchronization
- Unique to Packet Switched Networks (PSN)
- Stresses clock recovery mechanism leading to reduced synchronization accuracy

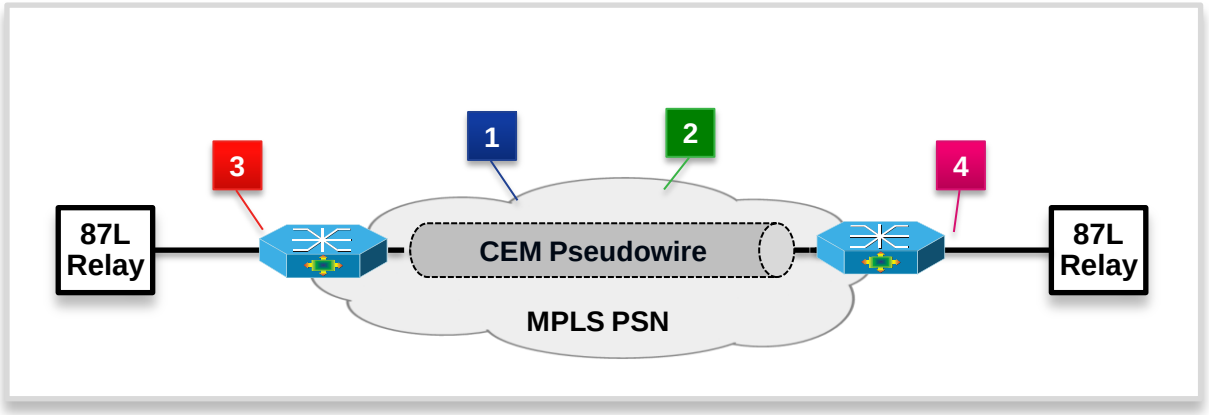
Latency Asymmetry & PDV impact all packet based two-way time transfer protocols, like for example, IEEE 1588 PTP commonly used in Service Provider WAN, and more recently in IEC 61850 Substation LANs

Circuit Emulation Over Packet Switched Networks

- Most relays use synchronous protection interfaces
  - G.703, EIA-422, X.21, V.35, T1/E1, C37.94 etc.
  - Developed over time to align with TDM communication equipment at substations.
- Relay interfaces line-time from attached PSN nodes
- PSN nodes can be frequency synchronized using
  - ITU-T SyncE (Physical Layer)
  - IEEE 1588 PTP (Packet based)
- PSN must support Circuit Emulation (CEM) to transport synchronous traffic
  - CESoPSN pseudowire
  - SAToP pseudowire

CEM involves accumulating fixed number of bytes of data from the synchronous interface, transporting them across the asynchronous PSN, and playing it out on the remote end at a fixed rate corresponding to the speed of the synchronous interface

Circuit Emulation - Sources of Delay



N x 64 kbps relay interface is slow-speed
compared to 1Gbps (or higher) network interface,
hence data has to be buffered at ingress and egress nodes

1) Fixed network delays:
   - Propagation latency (1msec / 200km of fiber)
   - Core link speed (1GE, 10GE)

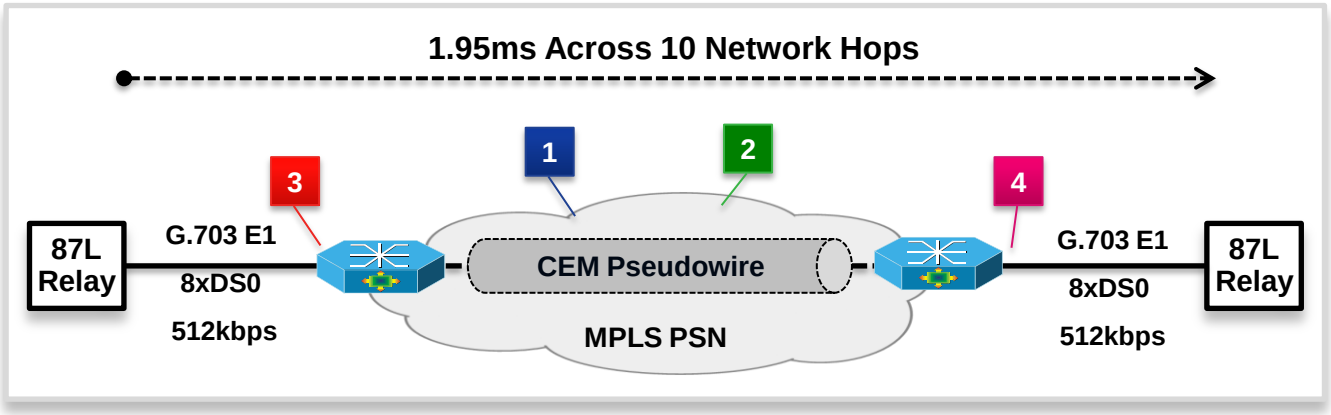
2) Variable network delays:
   - Switching latency at each network hop
   - Egress Queuing delay at each network hop

3) Ingress node delay:
   - Ingress packetization delay for CEM

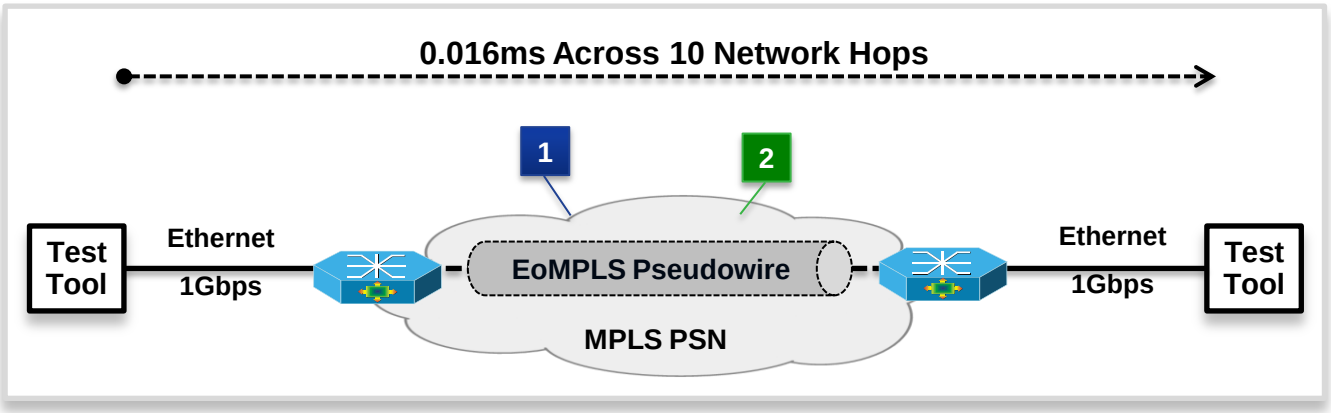
4) Egress node delay:
   - Egress Serialization Delay for CEM
   - De-jitter buffer delay for CEM

Latency

Latency for Relays with 512kbps Synchronous Protection Interface



Latency for Relays with 1Gbps Ethernet Protection Interface



- Transit node switching latency is 10-20us on hardware forwarding based platforms
- Buffering needed for CEM is largest contributor to delay
- CEM delay is dictated by relay interface speed
- CEM latency on hardware based forwarding platforms is well within delay budgets today
- Latency will become negligible as vendors move to Ethernet protection interfaces

Hardware forwarding based dataplane implementation of the platform is an important factor in achieving consistent latency targets

Latency Asymmetry

- Channel-based synchronization assumes equal Transmit and Receive latency
- PSNs relying on dynamic routing for reachability may have asymmetric forward and return paths
- Channel asymmetry can lead to latency asymmetry
  - Unequal hop counts, propagation delays, traffic load etc.
- MPLS based PSNs have mechanisms to traffic-engineer path symmetry
  - MPLS-TP bidirectional co-routed tunnels (static)
  - RSVP-TE strictly routed tunnels (dynamic)
- Traffic engineered symmetric paths may still have asymmetric latency due to queuing delays
  - The forward and return paths may have different traffic loads
  - QoS plays an important role in minimizing queuing delays

Hardware based QoS scheduling implementation of the platform is an important factor in minimizing queuing delays

Packet Delay Variation (PDV – “Jitter”)

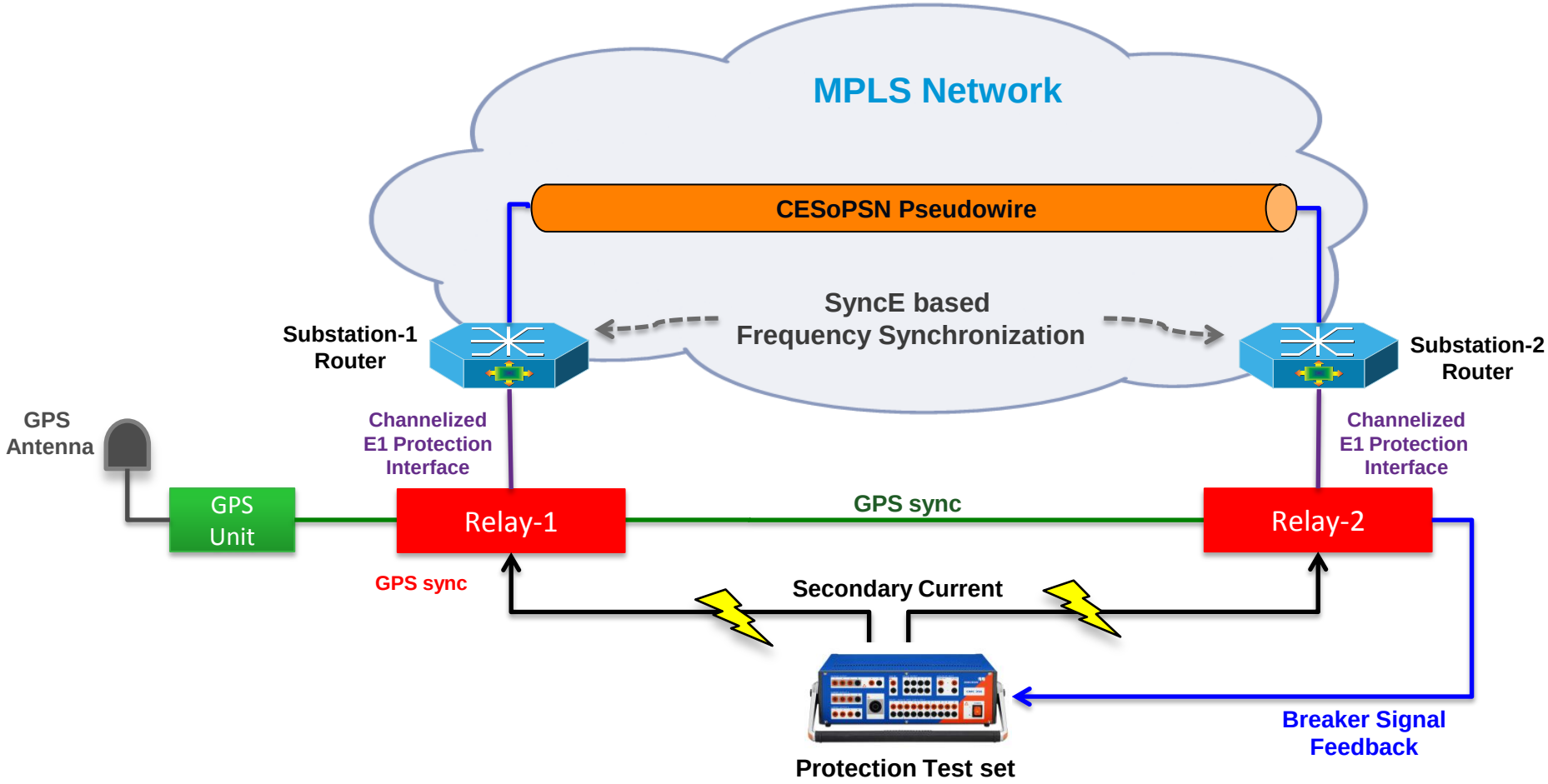
- Packet switching is based on the principal of statistical multiplexing
- Varying traffic loads at each hop along the path can lead to varying queuing delays
  - The resulting difference in one-way delay between packets in a flow is called PDV
- Jittered inter-arrival of time-stamped current samples leads to variation in *relayClockOffset* value
  - Impacts channel-based synchronization by stressing the clock recovery mechanism
- Relay (proprietary) clock recovery algorithm will dictate tolerance to network PDV
  - IEEE 1588 PTP (for example) compensates for PDV with sophisticated clock Servo algorithms to compute the precise offset correction for any timestamp before the local clock is corrected
- 87L datagrams must be mapped to QoS high-priority queue at each hop for expedited forwarding
  - Same best practice used for IEEE 1588 in Service Provider WANs for PTP Telecom Profile, and IEC 61850 Substation LANs for PTP Power Profile

Hardware based QoS scheduling implementation of the platform is an important factor in minimizing PDV resulting from queuing delays

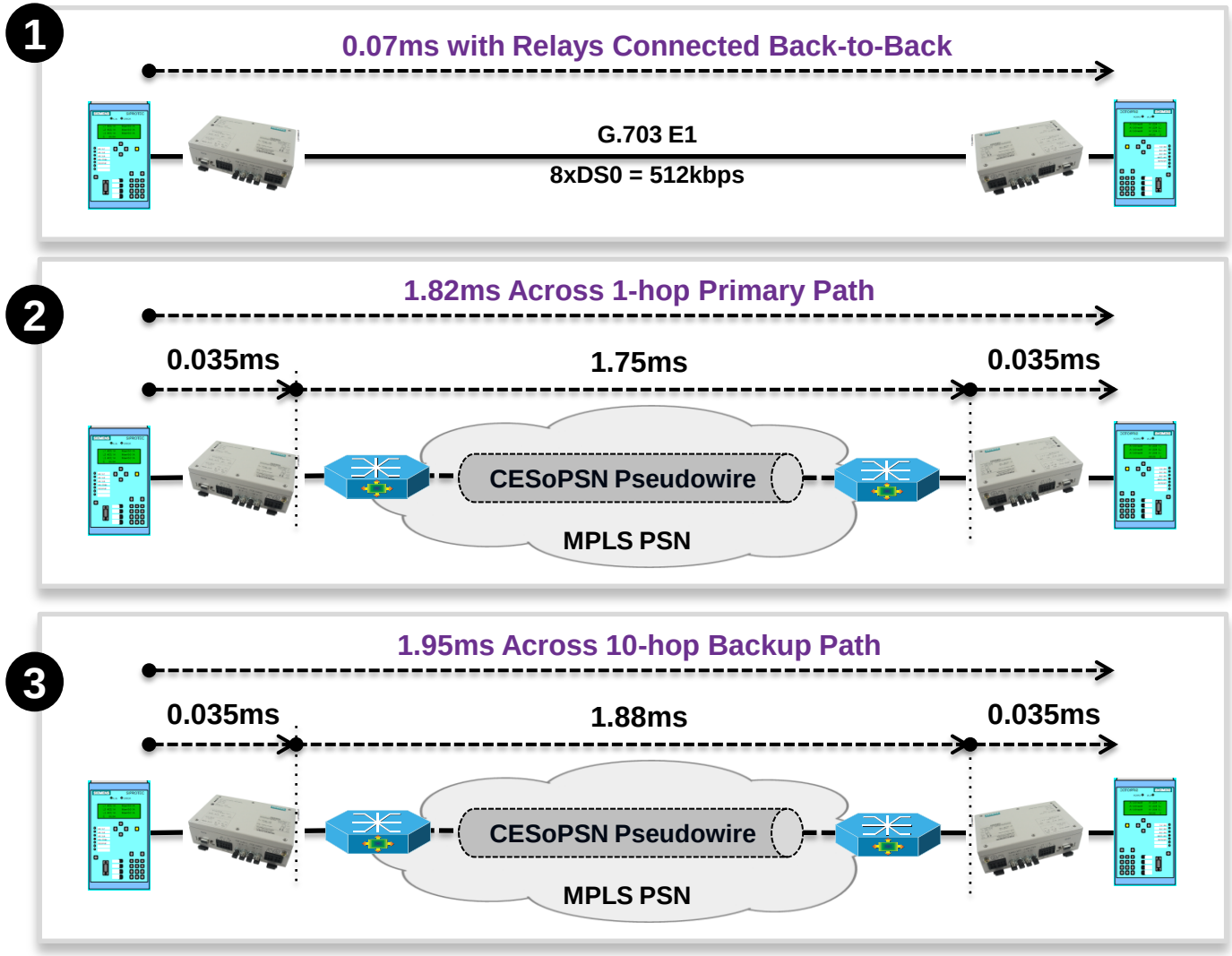
Recovery Mechanisms

- Two categories of sub 50msec failure recovery mechanisms
- Local-Protection
  - Switch traffic to a pre-signaled backup path at the point of failure
  - Typically used to protect all services flowing through the location being protected
- Path-Protection
  - Switch traffic to a pre-signaled backup path at the source, regardless of location of failure
  - Used to protect services flowing between two specific endpoints
- Some local-protection recovery mechanisms are topology dependent
  - May result in asymmetric forward and return repaired paths
  - These should only be used with GPS assisted schemes and are not suitable for channel-based synchronization
- Tolerance of 87L to channel failure recovery is dependent on sensitivity of relays to lost datagrams
  - Relays may operate in a degraded mode up to a threshold before relinquishing protection function
- Option to use relays with two protection interfaces
  - Datagrams traffic-engineered along divergent, non-fate-sharing paths

Test Setup


MPLS Network
CESoPSN Pseudowire
SyncE based
Frequency Synchronization
Substation-1
Router
Substation-2
Router
GPS
Antenna
GPS
Unit
Channelized
E1 Protection
Interface
Channelized
E1 Protection
Interface
Relay-1
GPS sync
Relay-2
GPS sync
Secondary Current
Breaker Signal
Feedback
Protection Test set

87L Communication Channel Latency over PSN



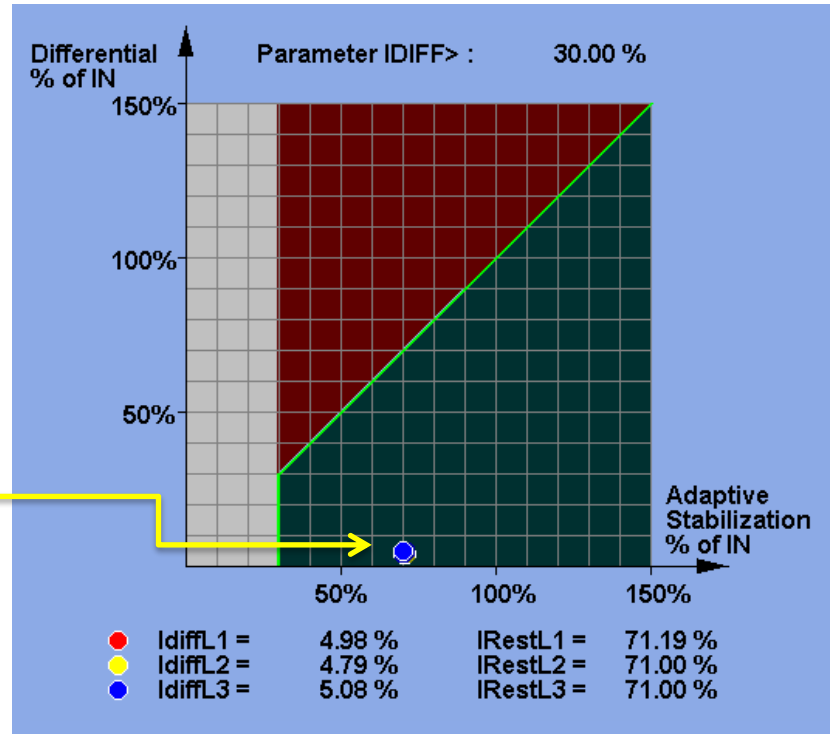
87L Relay

Relay Protection Interface Unit

MPLS Router

87L Operation over a Traffic Congested PSN

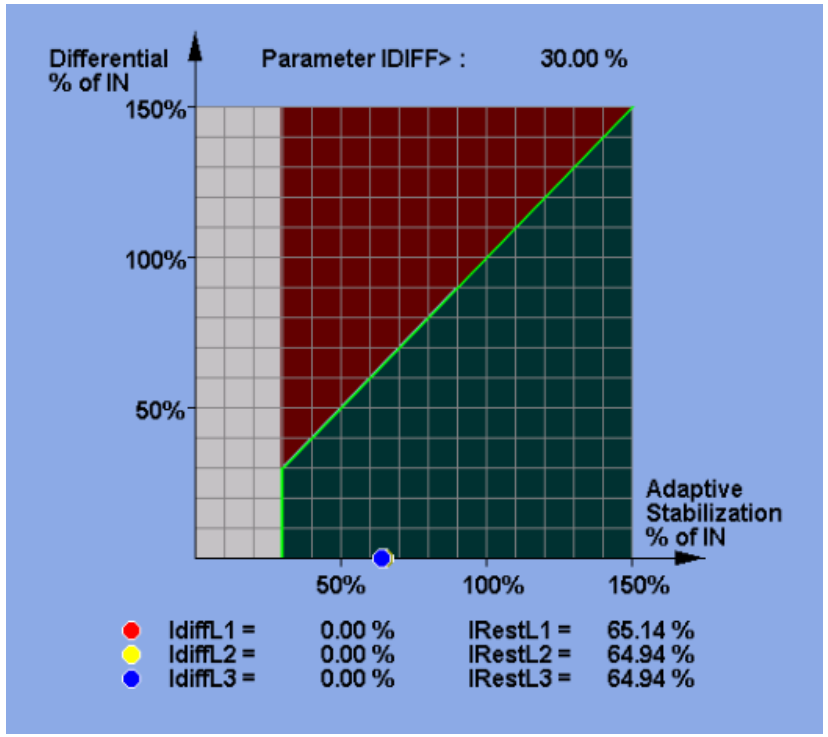
Relay Tripping Characteristic
with Channel-Based Synchronization



Very Stable
Even without GPS

Negligible differential current
Relays operating well below the 30% iDiff margin

Relay Tripping Characteristic
With GPS Assist



Zero differential current
Due to GPS based synchronization

Conclusions

- Carrier-grade PSNs can be reliably engineered to meet the constraints imposed by 87L
- The main factors consuming delay budget are relay protection interface types and speeds, and not the packet switched network itself.
- Path symmetry required by 87L schemes deployed using channel-based synchronization can be satisfied using MPLS traffic engineering techniques.
- PDV inherent in packet switched networks, can be effectively compensated for by efficient QoS mechanisms.

The level of determinism that a packet switched network can provide is dependent on the hardware implementation of the platforms that comprise the network

Questions?