Balancing DER Ride-Through Requirements and System Protection A Utility Perspective




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QUANTA TECHNOLOGY

IEEE 1547 – What is it?

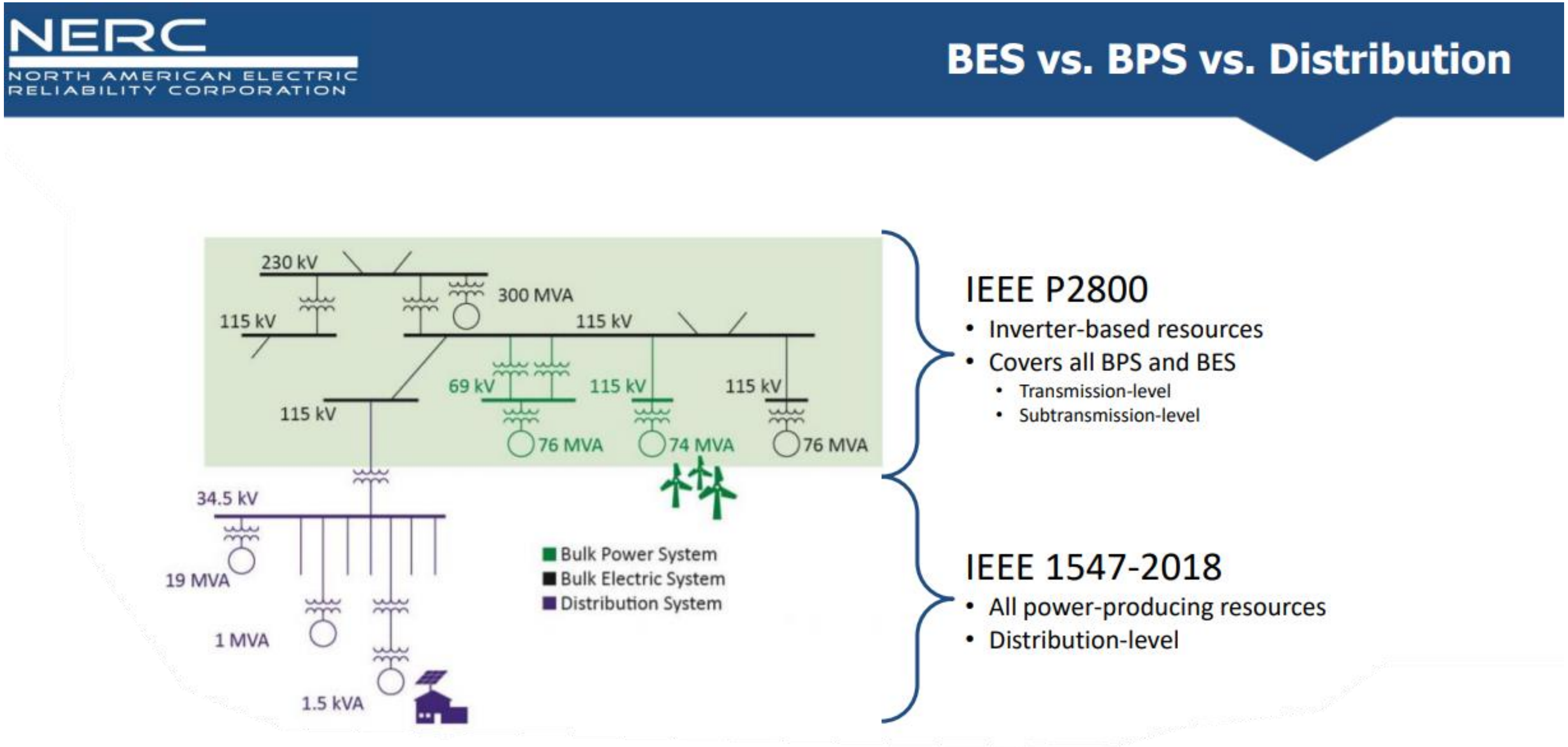
- The IEEE 1547 standard is the basis for a uniform standard for the interconnection and interoperability of distributed energy resources with electric power systems.
- It provides requirements relevant to the interconnection and interoperability performance, operation and testing, and, to safety, maintenance and security considerations.
- This standard focuses on the technical specifications for, and testing of, the interconnection itself, and not on the types of the DER technologies.
- The standard aims to be technology-neutral, although acknowledges that the technical attributes of DER and the types and characteristics of EPSs do have a bearing on the interconnection requirements.

Outline of IEEE 1547-2018

1. Overview
2. Normative references
3. Definitions and acronyms
4. General interconnection technical specifications and performance requirements
5. Reactive power capability and voltage/power control requirements
6. Response to Area EPS abnormal conditions
7. Power quality
8. Islanding
9. DER on distribution secondary grid/area/street (grid) networks and spot networks
10. Interoperability, information exchange, information models, and protocols
11. Test and verification requirements

What about Transmission vs. Distribution DER Standards?

IEEE 2800 vs. IEEE 1547 standards

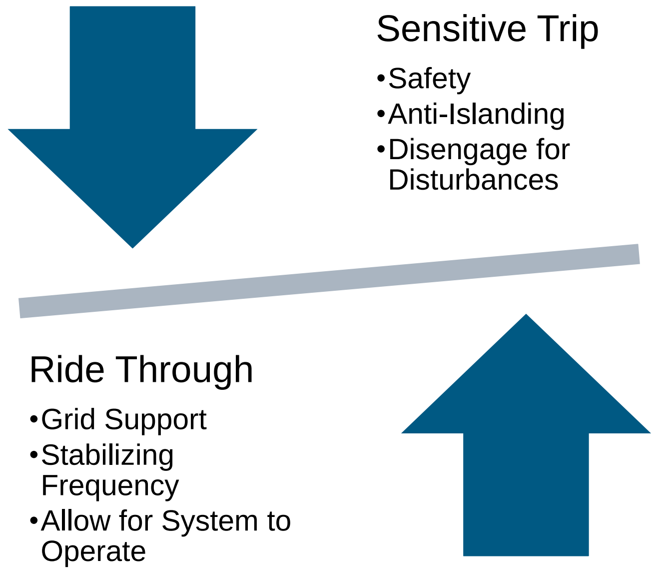


[The Next Perfect Storm (naruc.org)](https://www.naruc.org)

IEEE 1547 Evolution of Grid Support Functions

IEEE 1547-2003	• **Shall** NOT actively regulate voltage • **Shall** trip on abnormal voltage/frequency.
IEEE 1547a-2014 (Amendment 1)	• **May** actively regulate voltage • **May** ride-through abnormal voltage/frequency • **May** provide frequency response (frequency droop).
IEEE 1547-2018	• **Shall** be capable of actively regulating voltage • **Shall** be capable of frequency response • **Shall** ride-through abnormal voltage/frequency • **May** provide inertial response

IEEE 1547 – Grid Support



Ride-Through
Ability to withstand voltage or frequency disturbances inside defined limits and to continue operating as specified.

Impacts of Transmission Disturbances - Voltage

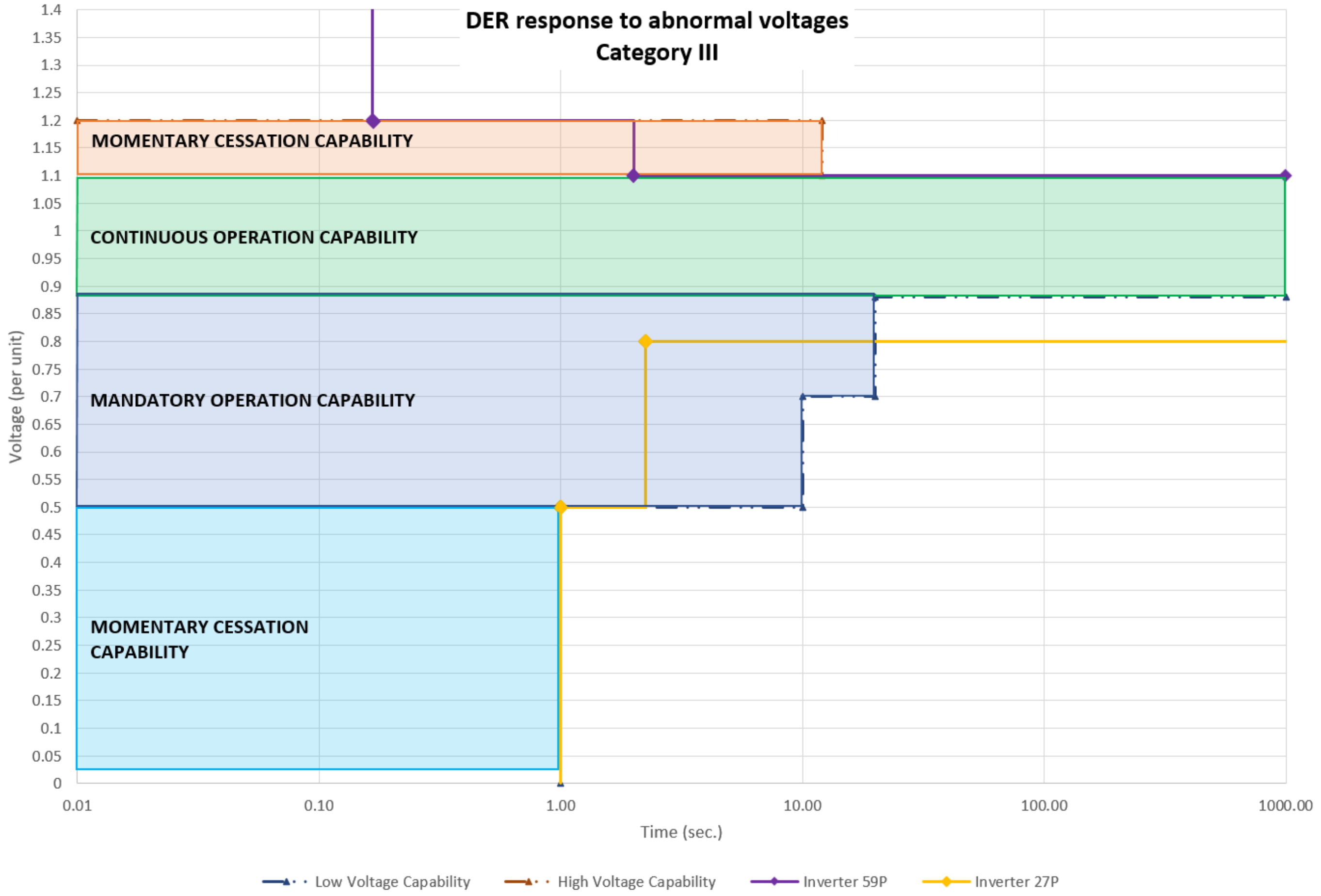
- Transmission faults can depress distribution voltage over very large areas
- Overly sensitive DER voltage protection can result in widespread loss of DER generation.
- DER response to Transmission events could result in further system degradation

Impacts of Transmission Disturbances - Frequency

- System frequency is defined by the balance between load and generation.
- Frequency is nearly the same across entire interconnection; all DERs can trip simultaneously during disturbance.
- Impact is the same whether or not DER is on a high-penetration feeder. *

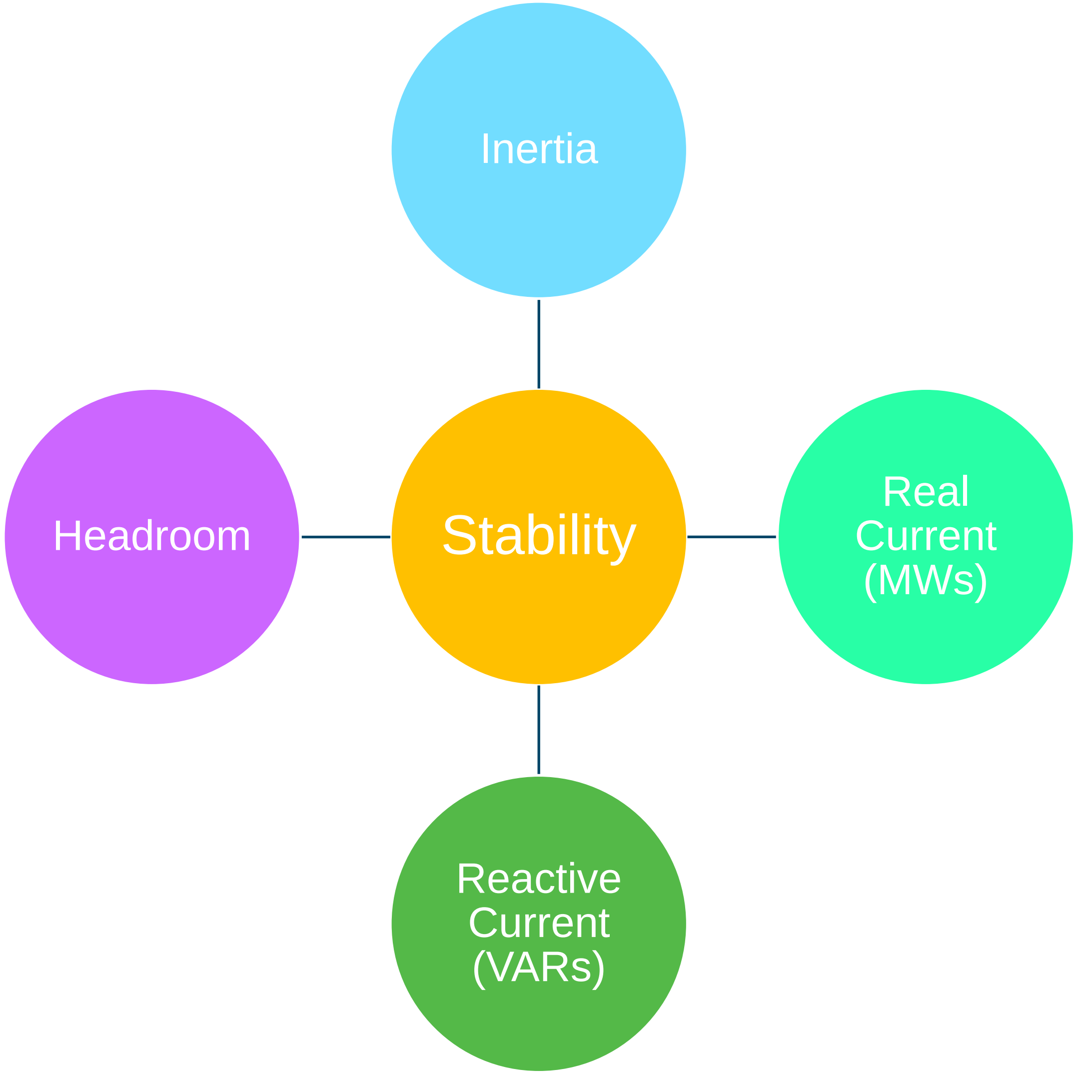
*Credit to Dr. Jens Boemer

Voltage Ride-Through of Inverter Based DER (Utility Scale DER >=1MW)

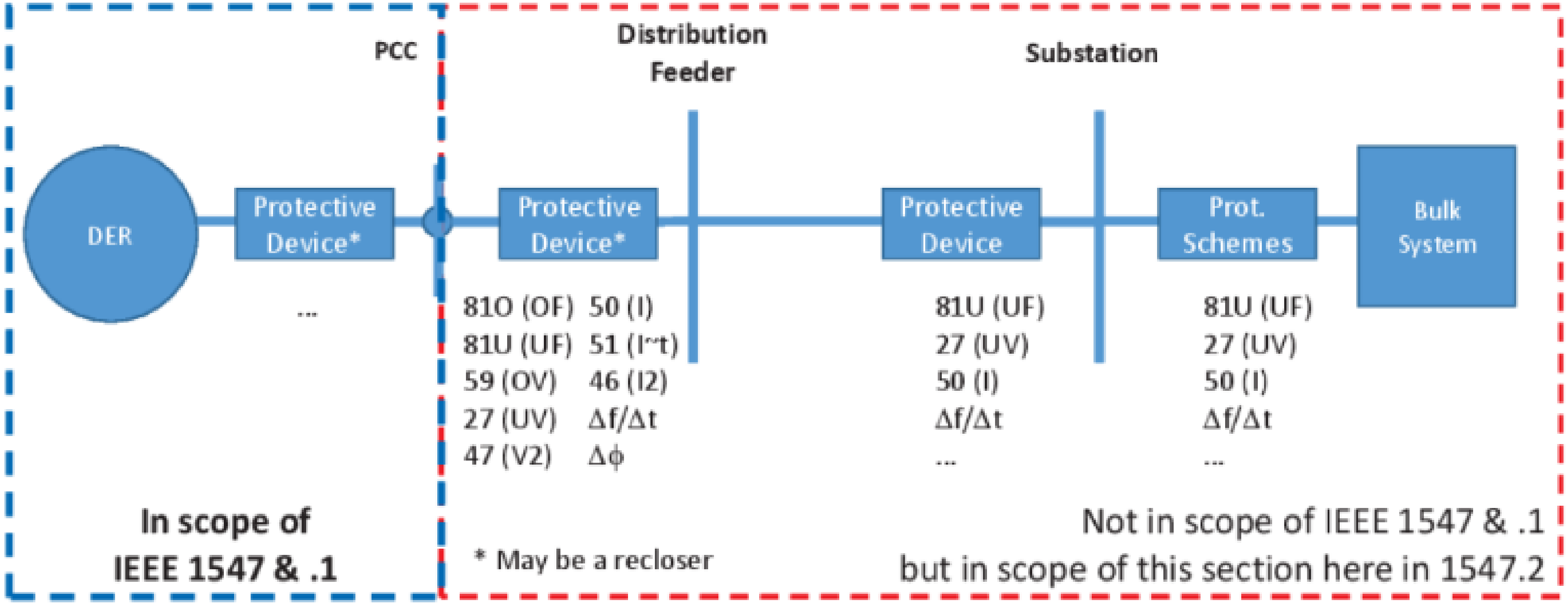


- Need to determine the Normal Operating & Abnormal Operating Capability that is desired for the Inverter Based DER Generators
  - The deep sag ride-through is important and determined the need for Category III capability
- Inverter Voltage/Frequency Clearing Times:
  - The OV1 clearing time should be evaluated for balancing system recovery time vs overvoltage exposure
  - The OV2 clearing time is fixed per the standard
  - The UV1 clearing time should be evaluated to balance delayed system recovery vs undervoltage exposure
  - The UV2 clearing time should be evaluated to coordinate with transmission system breaker clearing time, to allow the transmission system to manage Bulk Electric System (BES) disturbances.
  - The UF clearing times should be aligned with transmission schemes to provide the best support of the Bulk Electric System (BES).
  - The OF clearing times could be evaluate if the default values of the standard are acceptable.

Power System Stability



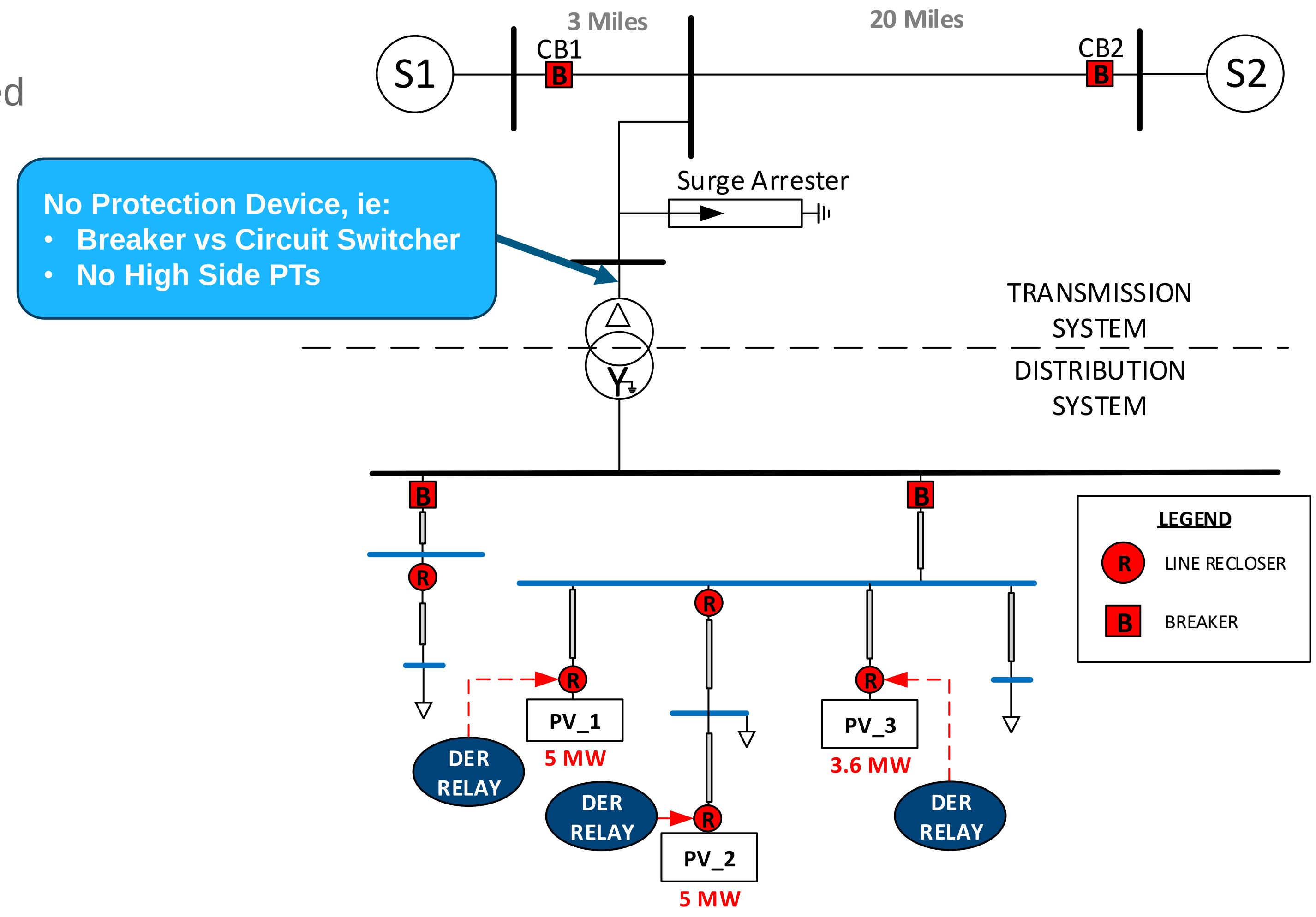
Ride-Through Flaws



- The relay at the interconnecting point between the DER site and the interconnecting system is out of scope of IEEE 1547
- Ride-through requires a lot more than just voltage and frequency protection

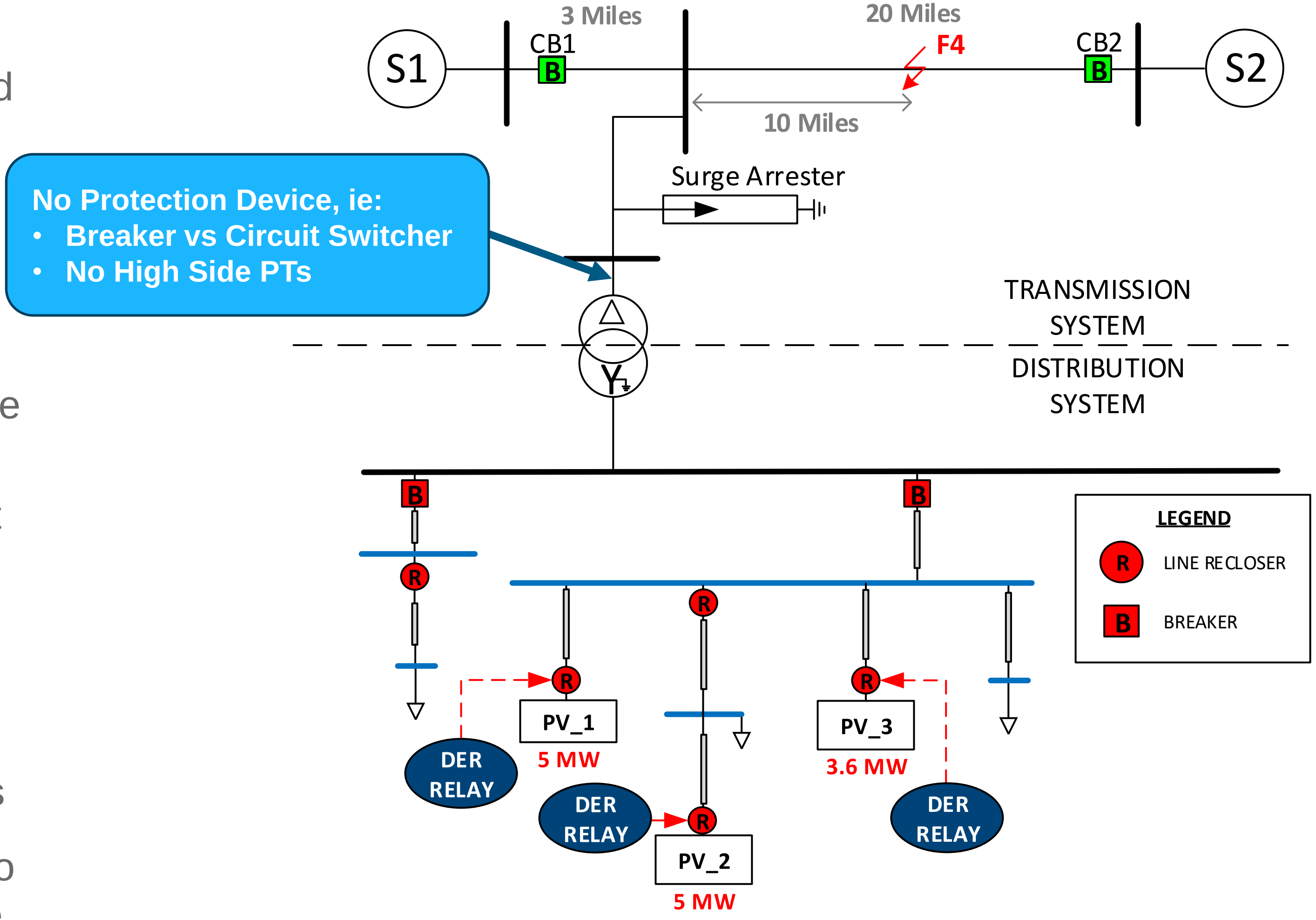
Ride Through Challenges

- Legacy substation design practices were based on one-way power flow



Ride Through Challenges

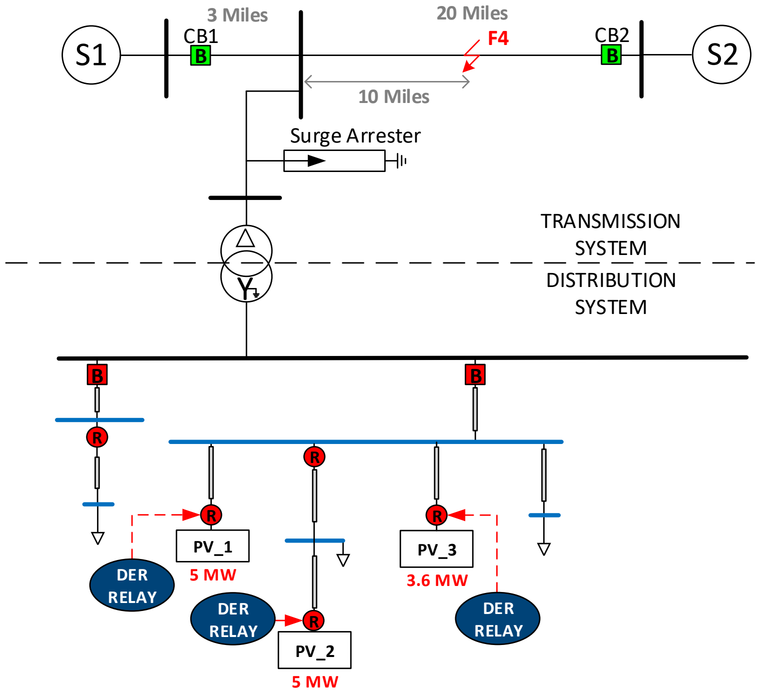
- Legacy substation design practices were based on one-way power flow
- Faults on Local Transmission system create a challenge when implementing DER Ride Through settings
  - Potential for Ground Fault Transient Overvoltage (GF-TOV) on Transmission line after breakers clear fault
  - Lack of existing infrastructure to implement solution on Transmission system
  - GF-TOV can damage surge arresters or other power equipment
- Evaluate protection scheme at Distribution system DER to detect Transmission SLG faults
  - Scheme is difficult to implement due to many factors drive system impedance

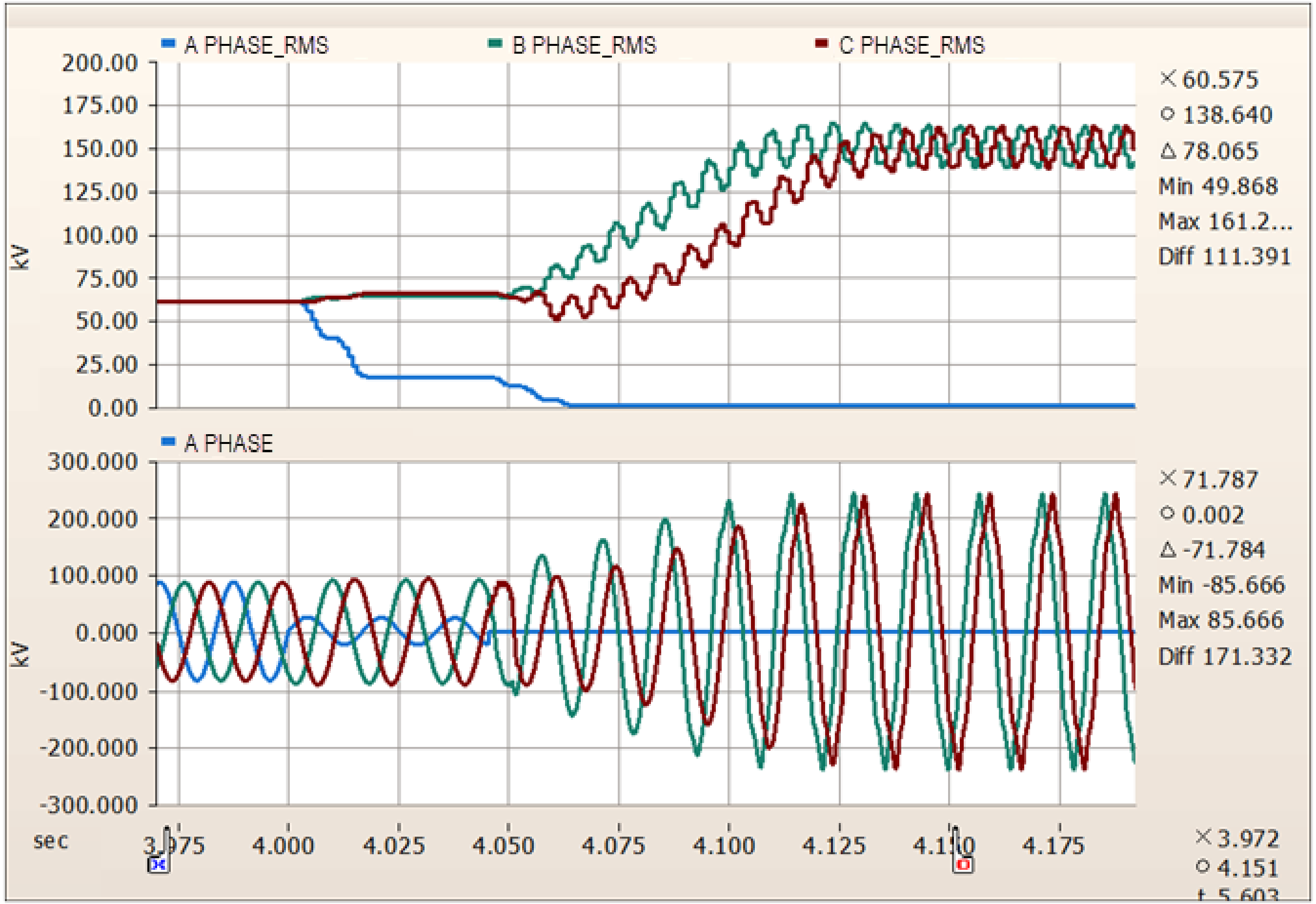


GROUND FAULT INDUCED TOV

GROUND FAULT TOV

- TRANSMISSION SINGLE LINE TO GROUND (SLG) FAULTS ARE OF MOST CONCERN
- TOV MAGNITUDE IS DEPENDENT ON LOAD TO GENERATION RATIO





Passive Voltage Protection

Primary method of system level fault detection for IBR based DERs

Phase Overvoltage (59P)

Phase Undervoltage (27P)

Passive Voltage Protection

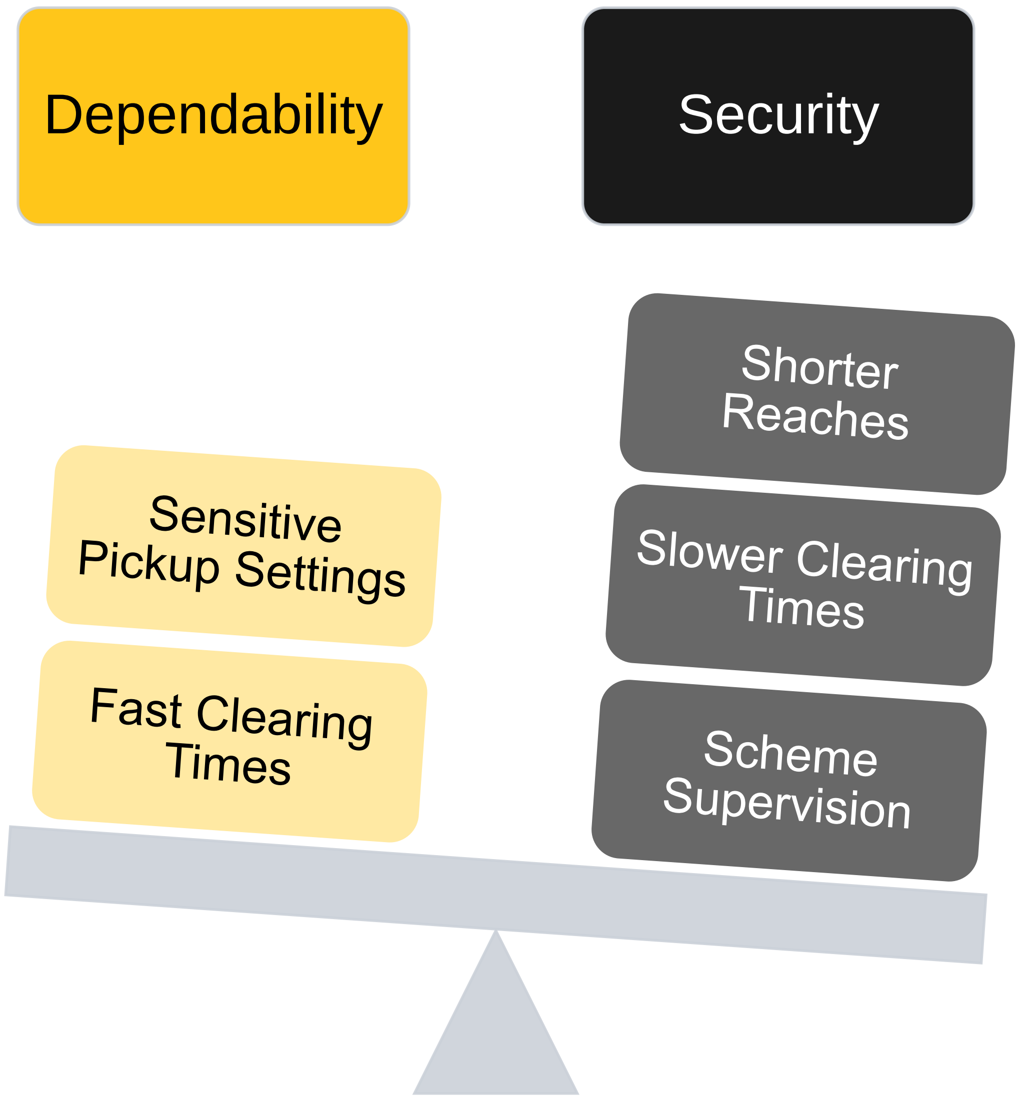
Pros

- Very Dependable
- Easy to deploy
- Very reliable for a synchronous generation-based system

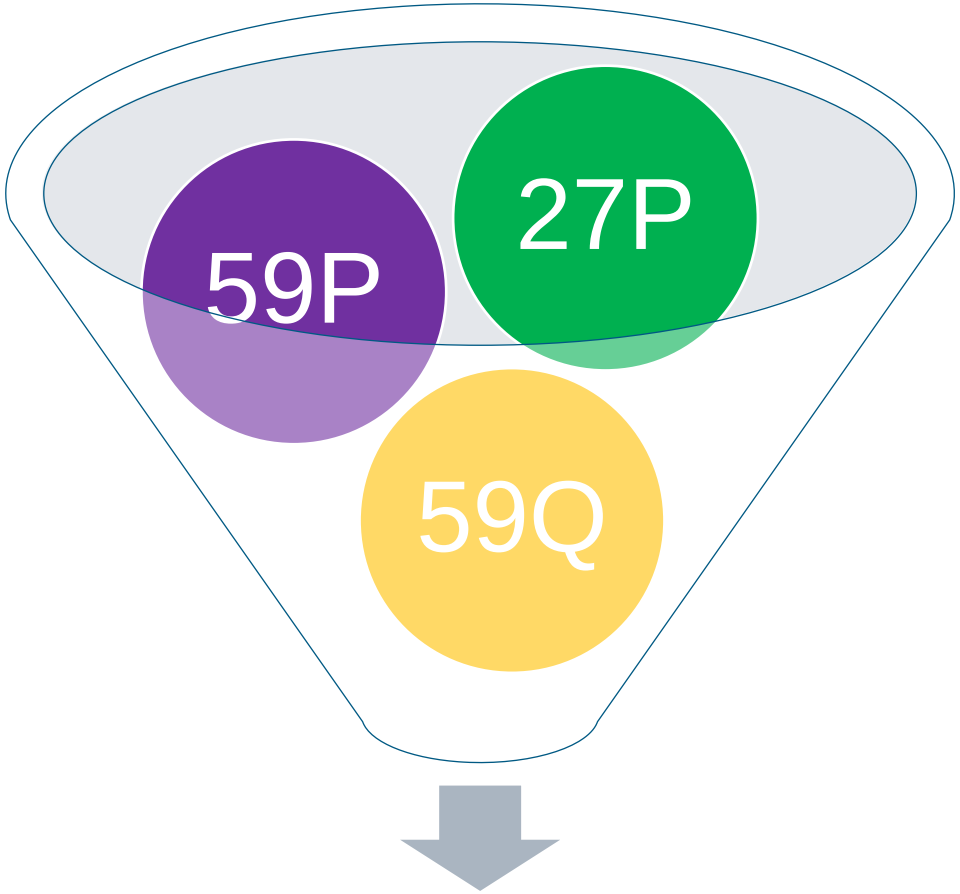
Cons

- Security Limitations
- Difficult to coordinate with relays within the distribution system

General Protection Performance



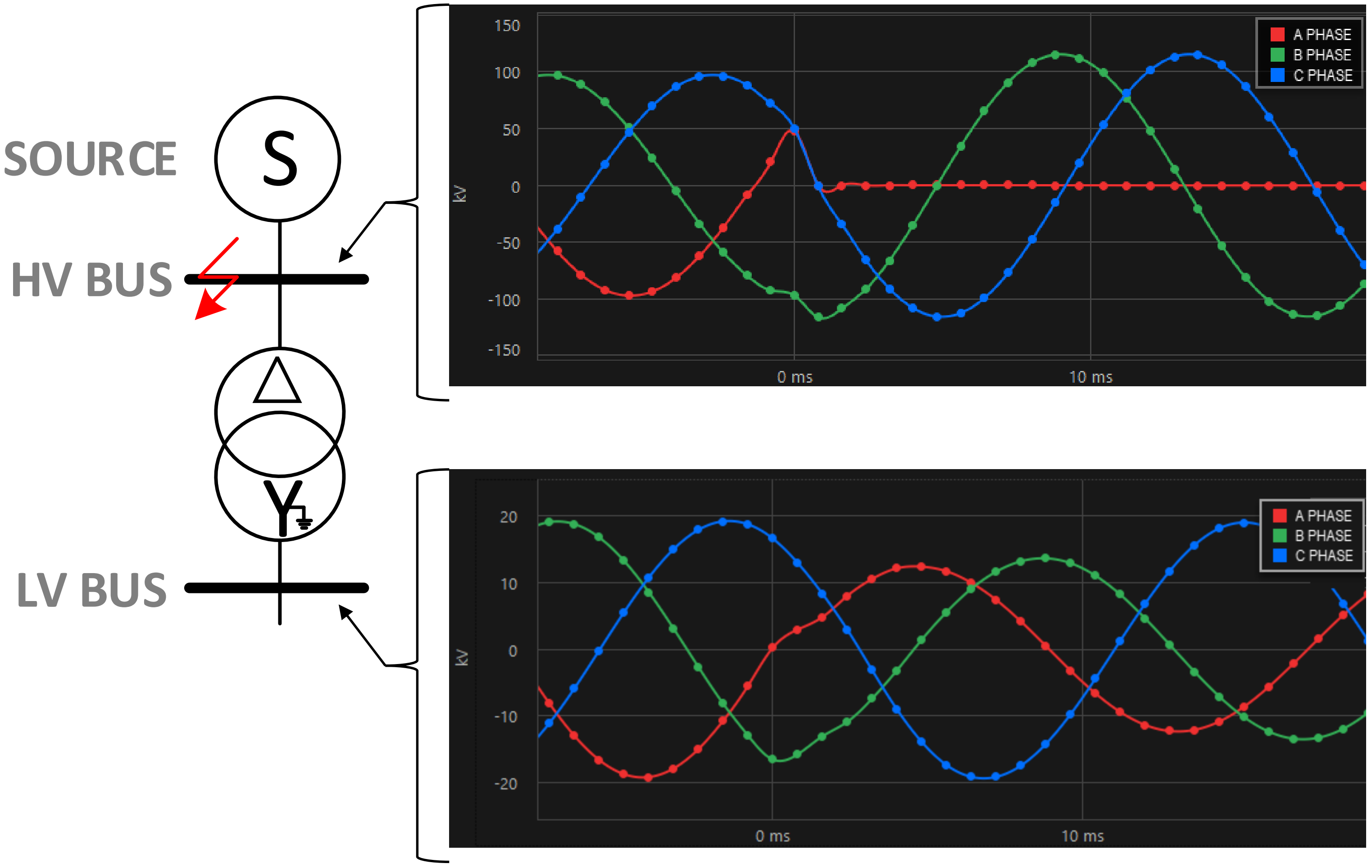
Voltage Based Signature Schemes



Fault Signature Schemes

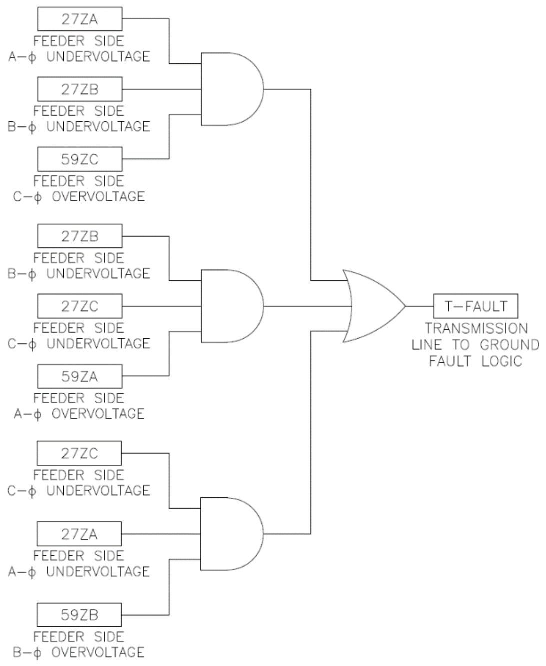
TRANSMISSION SLG VOLTAGE SIGNATURE

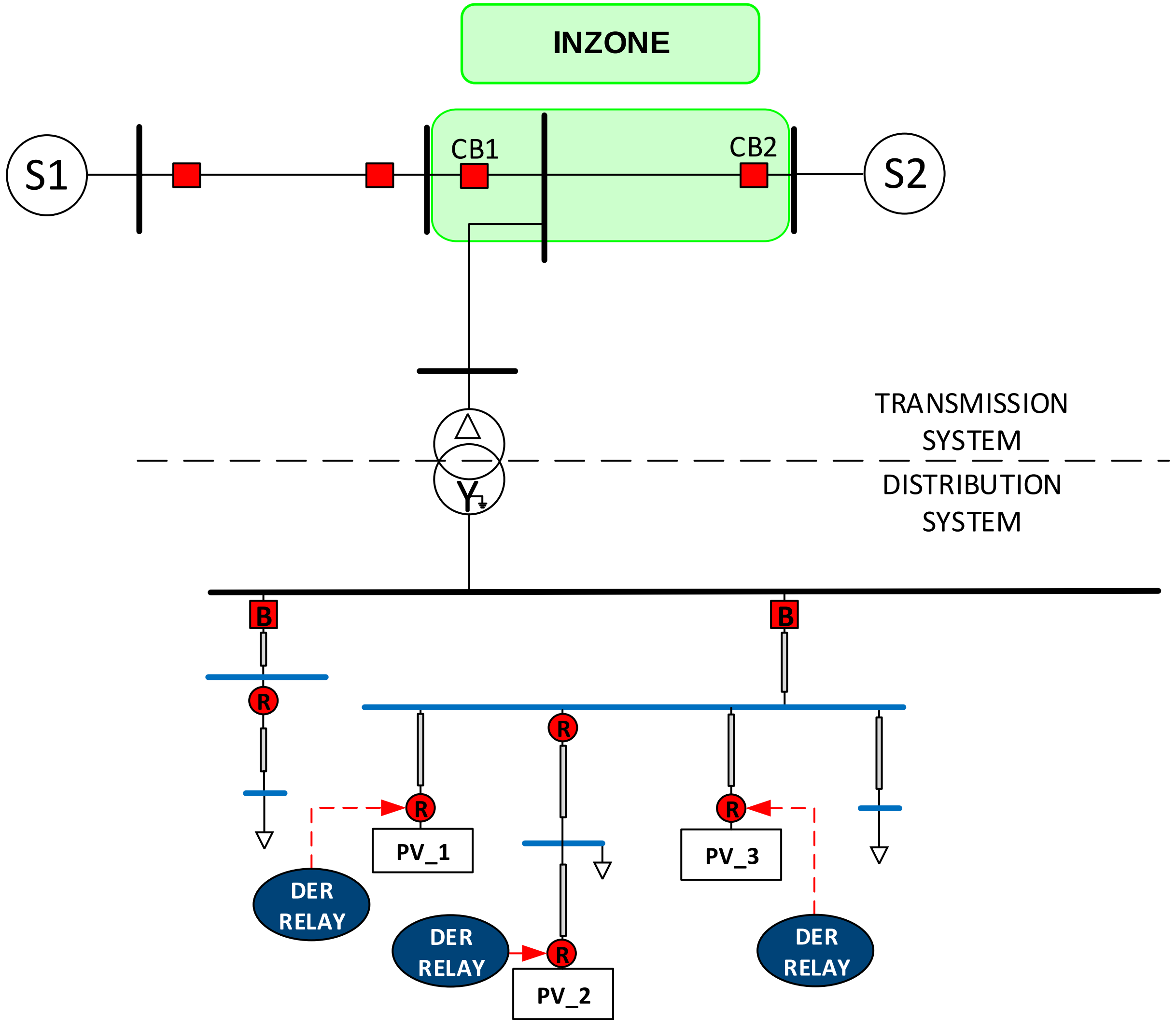
- Single line to ground (SLG) fault on HV side of Delta Wye-Grounded transformer is reflected as two phases low on LV side
- This logic can be used to as a sophisticated voltage scheme to detect faults (T-FAULT)
  - Signature is only present while Transmission system is connected
  - T-FAULT logic is susceptible to detecting faults that are beyond the local transmission line breakers



T-FAULT Scheme Challenges

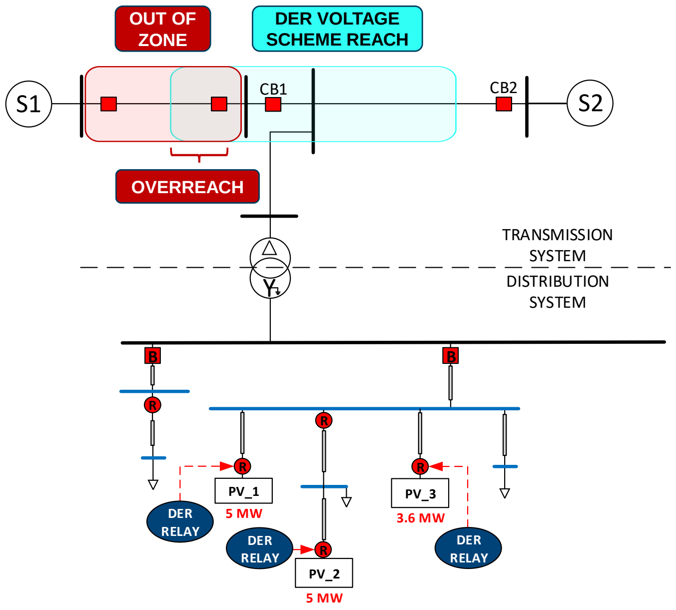
- It appears that the performance of sophisticated voltage schemes are sensitive to system parameters:
  - Loading conditions
  - DER generation levels
  - Distance from T/D substation

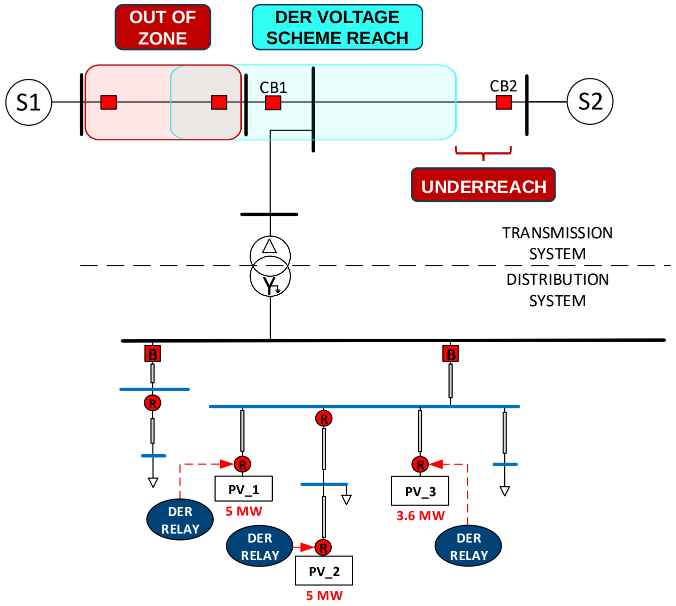




T-FAULT Scheme Challenges

- The asymmetry that is present in many systems limit the scheme's reach and results in misoperations
- The T-FAULT logic voltage setpoints need to be evaluated for each site
- The overreach has the potential to impact ride-through performance and the underreach signifies that the scheme may not be dependable
- The overreach has the potential to impact ride-through performance and the underreach signifies that the scheme may not be dependable





Voltage Based Signature Schemes

Pros

- Can detect faults along the tapped transmission line
- Can isolate the DERs very quickly

Cons

- Must overreach for 100% protection. This makes the scheme susceptible to misoperations
- Relies in the transmission connected synchronous generation to reliably operate
- Schemes are complicated and difficult to set
- Performs very poorly on asymmetrical transmission lines
- Prone to misoperate for faults along adjacent feeders
- Dependent on system parameters. As system topology and variables change the pickups may require modifications

Frequency Protection

Past IEEE 1547 Versions

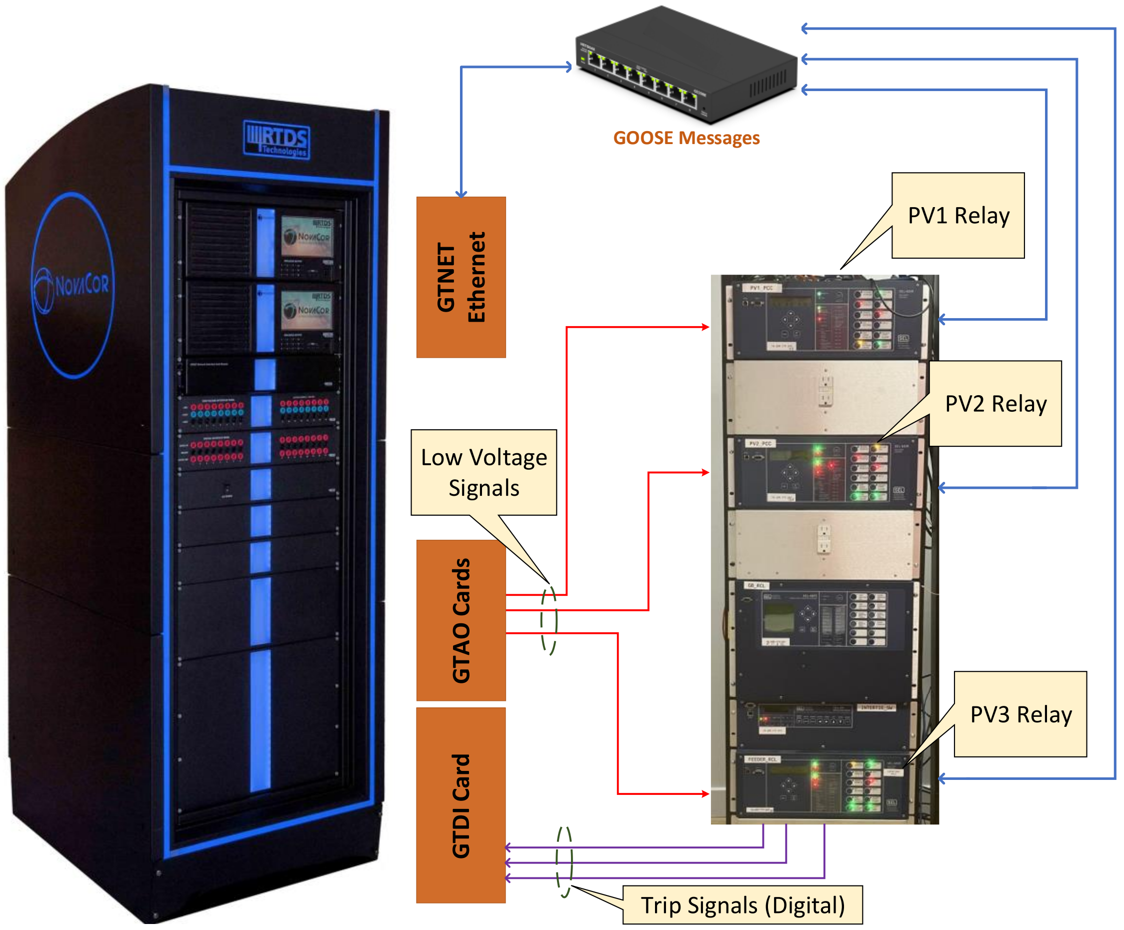
Anti-Islanding Bias

IEEE 1547-2018

Frequency Protection Ride-Through Bias

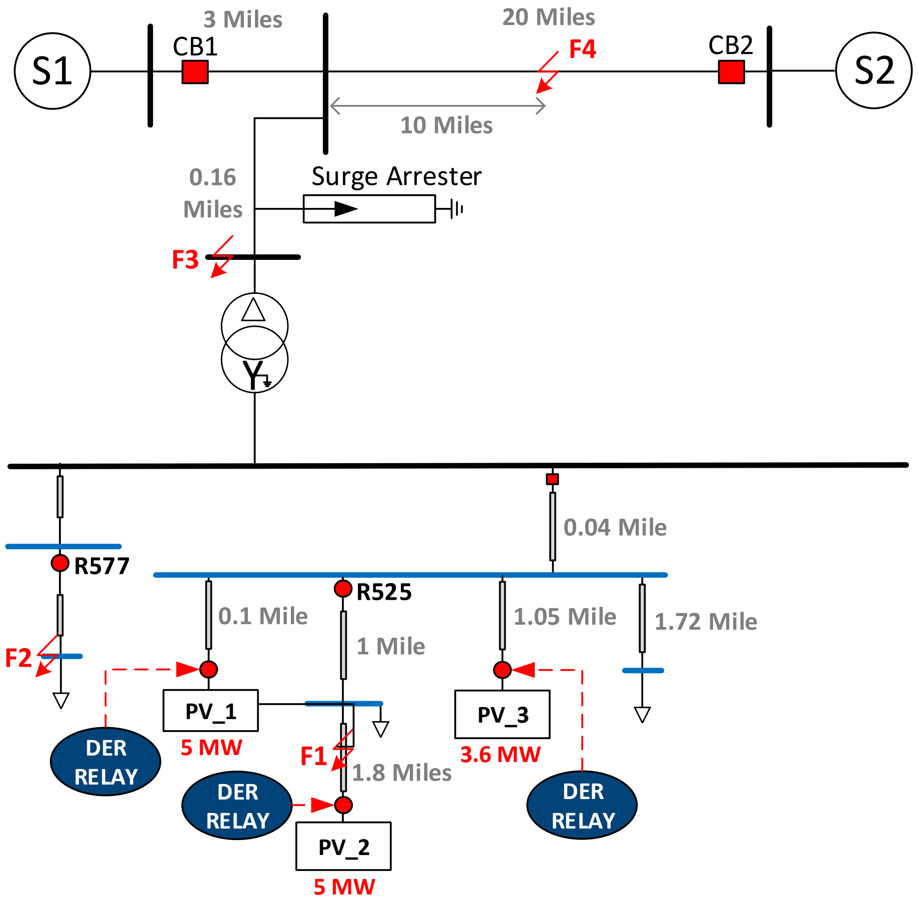
TESTBED SETUP

- The laboratory setup employed Control Hardware in Loop (CHIL) to perform closed-loop testing.
- The devices under test are the DER site protective relays
- The relays are interfaced with the Real Time Simulator utilizing:
  - Analog Output Cards (GTAO)
    - Voltage and Current to Relay
  - Digital Input Cards (GTDI)
    - Recloser Trip Signals to RTDS
  - Network Protocol Interface (GTNET)
    - Monitor Various status during testing



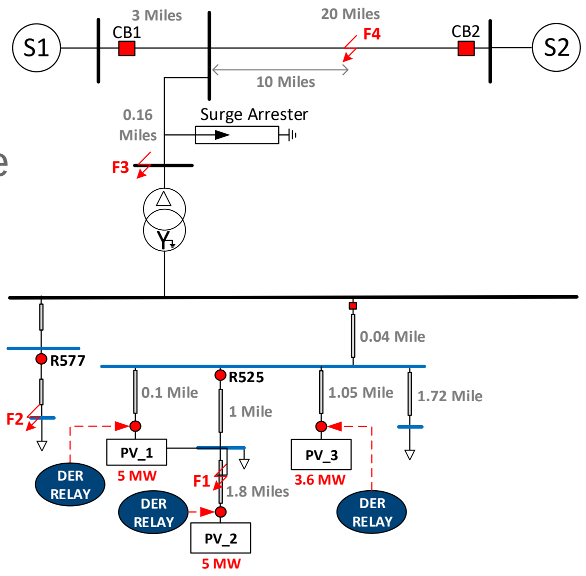
TEST SCOPE

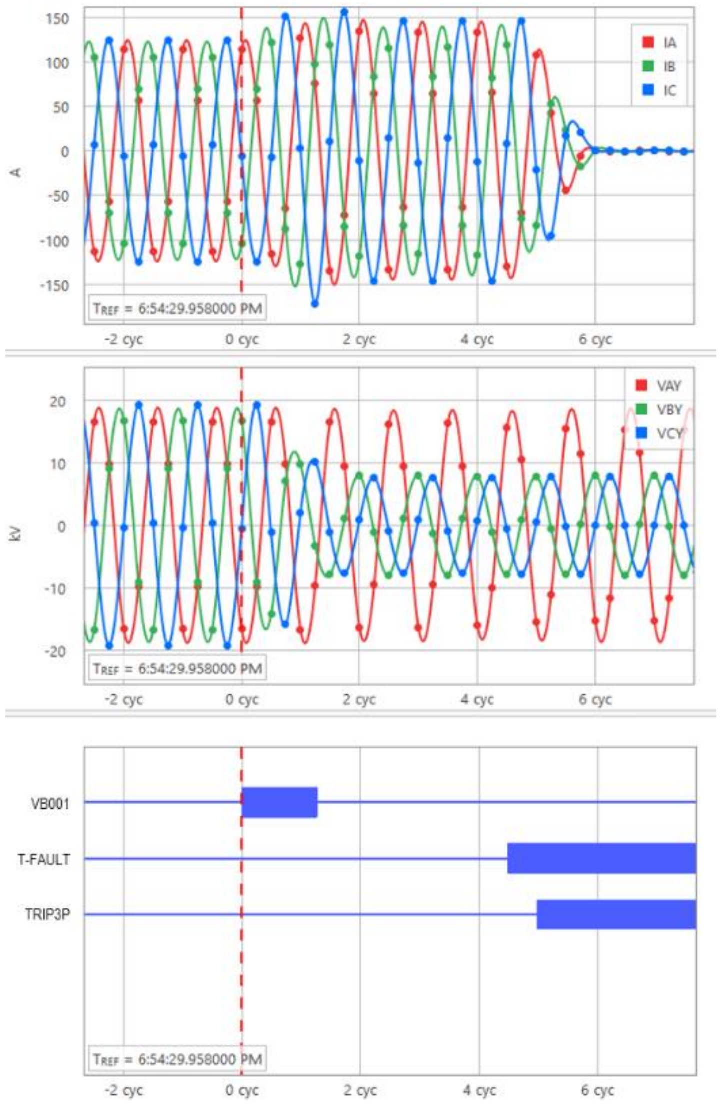
- The testing scope included a benchmark protection scheme (DER-RT) and the T-FAULT scheme
  - Various fault locations were selected for evaluation
  - Various fault types were evaluated for each fault location
  - Loading was varied for fault scenarios
- DER-RT the protection logic that is implemented at a Point of Common Coupling (PCC) recloser that consists of:
  - Passive Elements
    - Based on IEEE 1547-2018, Section 6
  - Sequence Component Elements
    - To detect faults on the Electric Power System (EPS)
  - Directional Overcurrent Elements
    - To detect faults within the DER site



TEST Results – BCG Fault at F1

- Ideal response for Line-Line-Ground Fault at F1 is reclosers R525 and PV_2 trip to isolate the fault and all other protective devices should not operate
- DER-RT protection scheme
  - PV_2 Trips on undervoltage
  - R525 Trips on overcurrent in 6.3 cycles
- T-Fault logic
  - PV_2 Trips on zero-sequence overvoltage
  - R525 Trips on overcurrent in 6.6 cycles
  - PV_1 and PV_2 Trip on T-FAULT logic

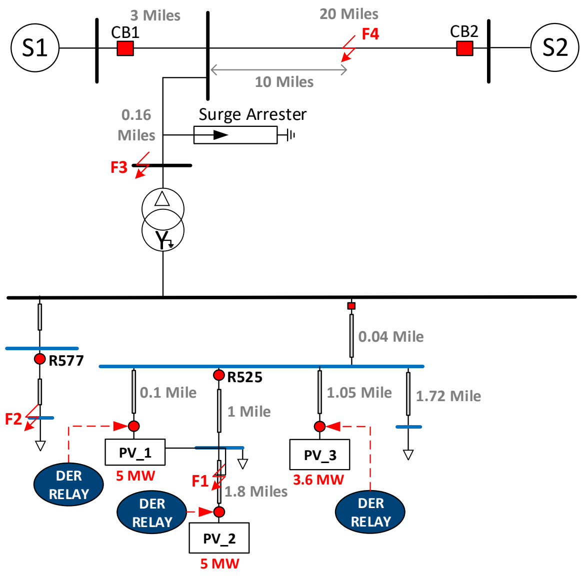


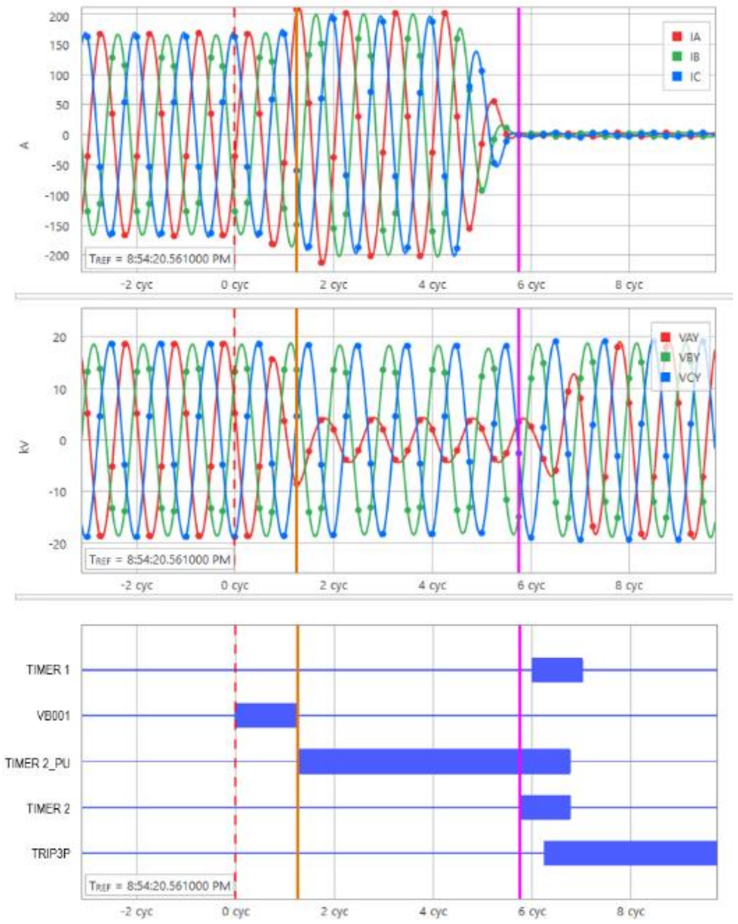


COMTRADE Event File for a Fault at F1 (PV3, voltage signature based protection)

TEST Results – AG Fault at F2

- Ideal response for Line-Ground Fault at F2 is recloser R577 to isolate the fault and all other protective devices should not operate
- DER-RT protection scheme
  - Timer 2 (zero sequence overvoltage) has a 10 cycle delay
  - R577 Trips on overcurrent in ~6 cycles
  - PV_1, PV_2, and PV_3 ride-through
- T-Fault logic
  - Timer 2 (zero sequence overvoltage) is intentionally set to miscoordinate with a 4.5 cycle delay
  - R577 Trips on overcurrent in ~6 cycles
  - PV_1, PV_2, and PV_3 Trip ride-through

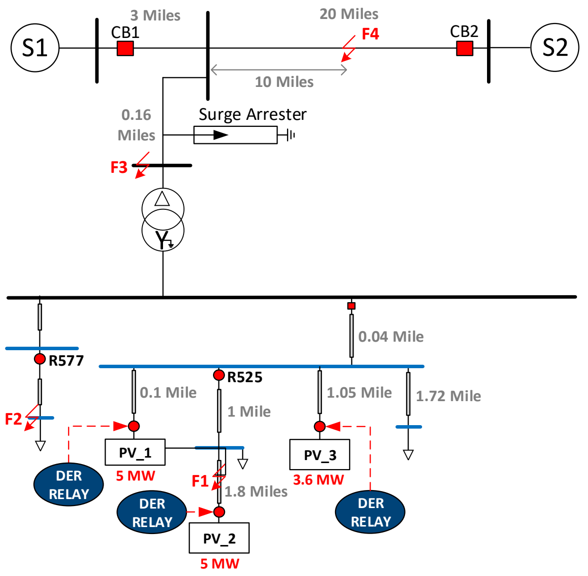


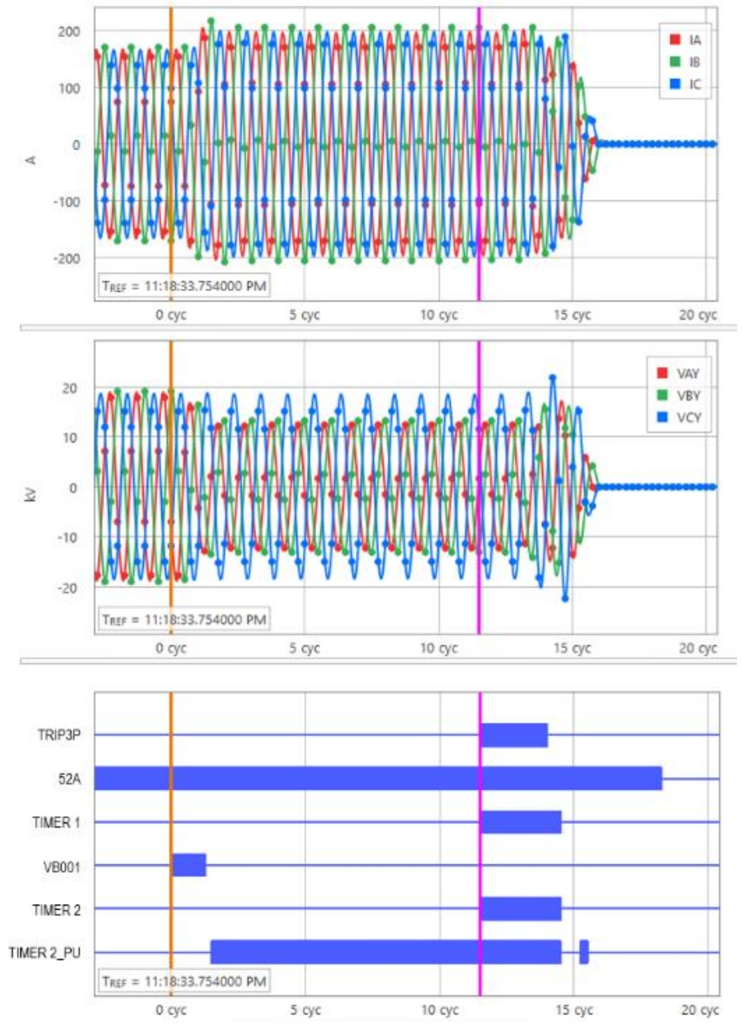


COMTRADE Event File for a Fault at F2
(PV1, voltage signature based protection scheme)

TEST Results – AG Fault at F3

- Ideal response for Line-Ground Fault at F3 is reclosers PV_1, PV_2, and PV_3 trip to stop injecting into the fault quickly prior to potential damaging TOV.
- DER-RT protection scheme
  - PV_1, PV_2, and PV_3 trip on Timer 2 (negative and zero sequence overvoltage elements) in ~12 cycles
  - Transmission Breakers CB1 and CB2 trip and clear the fault in ~13 cycles

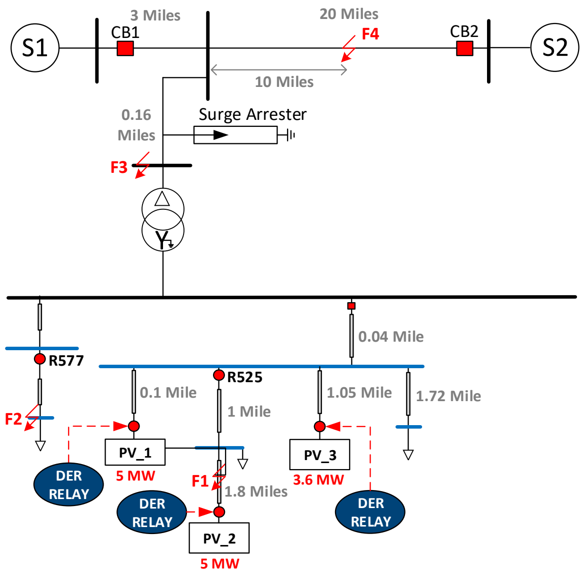


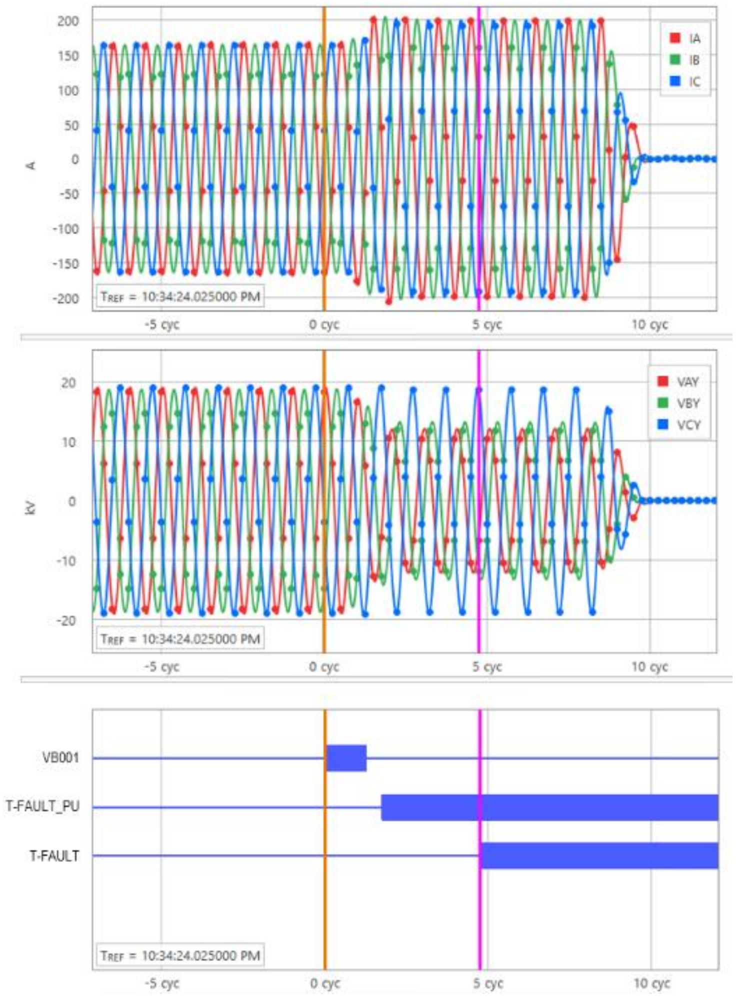


COMTRADE Event File for a fault F3 (PV1, DER-RT protection scheme)

TEST Results – AG Fault at F3

- Ideal response for Line-Ground Fault at F3 is reclosers PV_1, PV_2, and PV_3 trip to stop injecting into the fault quickly prior to potential damaging TOV.
- T-Fault logic
  - PV_1, PV_2, and PV_3 trip on T-FAULT logic in ~5 cycles
  - Transmission Breakers CB1 and CB2 trip and clear the fault in ~13 cycles

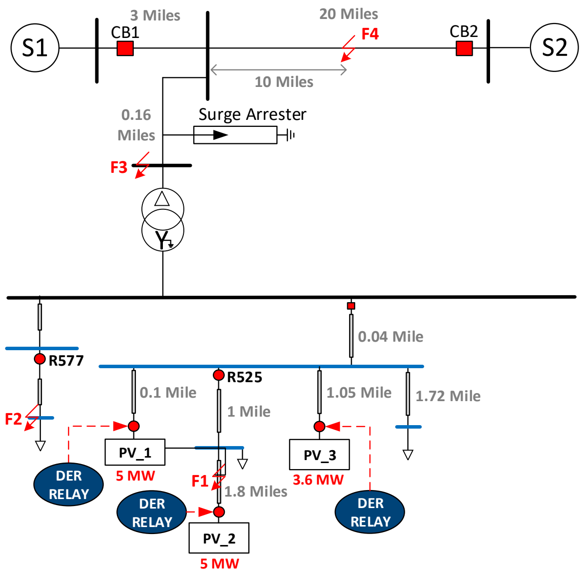


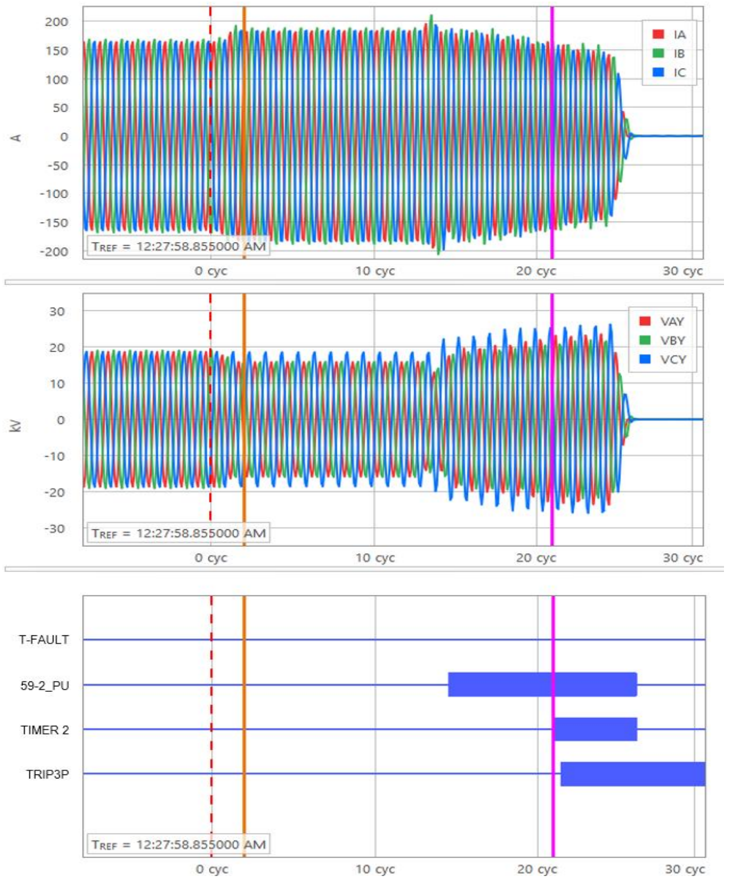


COMTRADE Event File for a fault F3
(PV1, voltage signature based protection scheme)

TEST Results – AG Fault at F4

- Ideal response for Line-Ground Fault at F4 is reclosers PV_1, PV_2, and PV_3 trip to stop injecting into the fault quickly prior to potential damaging TOV.
- DER-RT protection scheme
  - PV_1, PV_2, and PV_3 trip on Timer 2 (Level 2 overvoltage elements [59-2]) in ~23 cycles
  - Transmission Breakers CB1 and CB2 trip and clear the fault in ~13 cycles
  - Overvoltage condition develops until the DERs trip

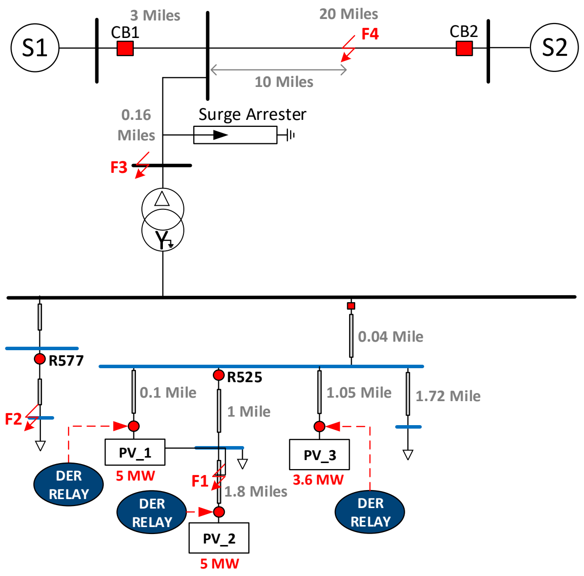


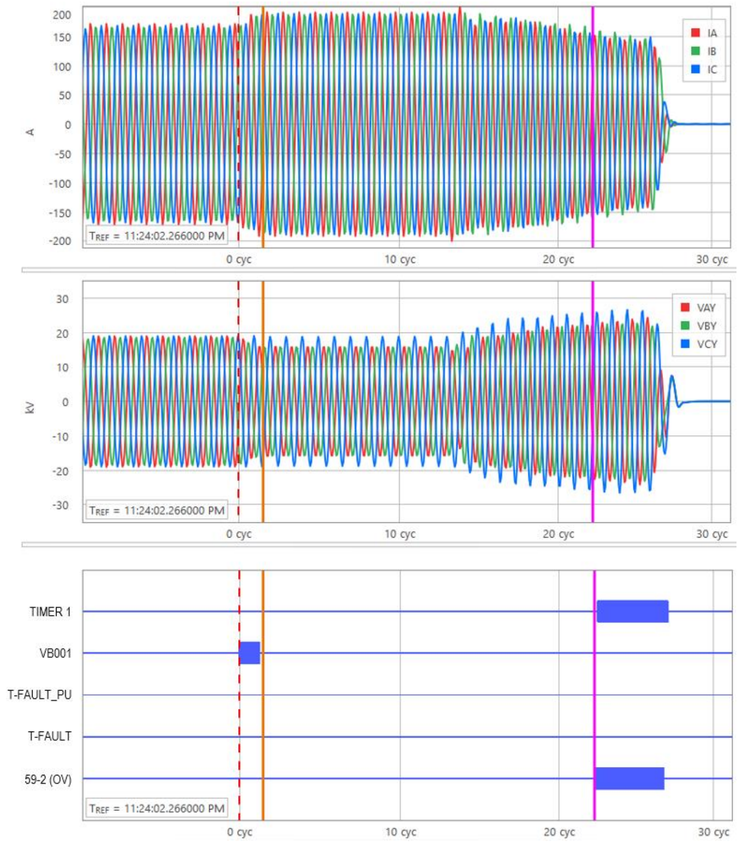


COMTRADE Event File for a fault F4 (PV1, DER-RT protection scheme)

TEST Results – AG Fault at F4

- Ideal response for Line-Ground Fault at F4 is reclosers PV_1, PV_2, and PV_3 trip to stop injecting into the fault quickly prior to potential damaging TOV.
- T-Fault logic
  - PV_1, PV_2, and PV_3 fail to trip (Misoperation)
  - Transmission Breakers CB1 and CB2 trip and clear the fault in ~13 cycles
  - Overvoltage condition develops until the DERs trip





COMTRADE Event File for a fault F4
(PV1, voltage signature based protection scheme)

Conclusion

- IEEE 1547 should investigate alternative forms of protection for abnormalities on the system. At minimum, they should create minimum fault current output requirements for DERs.
- High-speed fault signature schemes do not provide 100% reliable protection performance
- The IEEE 1547 “ride-through requirements” are flawed and outdated. As an industry, there is more work to be done in the realm of system stability and ride-through

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