Distance Relay Accelerator – Achieve Sub-cycle Operation Time

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Abstract- **It is well known that the operation speed of the phasor-based distance relay is limited by the phasor calculation window plus necessary prefiltering (for removing decaying DC in current signals and CVT transients in voltage signals) plus security delay to prevent overreaching. On the other hand, distance protection remains the primary protection on transmission lines and is required to increasingly improve its operation speed, especially for EHV or UHV applications. It typically requires sub-cycle operating time for the distance underreach zones and pilot scheme zones, to meet power system stability requirements.**

This paper presents a new algorithm, in which a distance relay accelerator is implemented to speed up distance elements operation. The accelerator runs in parallel with the regular full cycle Fourier based distance algorithm, but only runs for 3 cycles after it is armed upon fault occurrence, and then exits itself, to achieve optimal operation speed, security, and dependability requirements of the overall protection scheme.

This paper will present technical challenges and solutions for implementation and application of such distance accelerator algorithm. RTDS test results will be demonstrated and discussed in the paper.

Index Terms—**Distance Relay, Sub-cycle Operation Time, Transmission Line Protection.**

I. Introduction

Distance relays are widely used in transmission line protection due to its simplicity, economy and effectiveness, which use local voltage and current signals to provide selective and high-speed clearance of transmission line faults. Most distance protection algorithms in digital relays are based on fundamental phasors that are calculated via full cycle discrete Fourier transform (DFT), plus necessary prefiltering to remove decaying DC in current signals and CVT transients in voltage signals to improve the measurement accuracy, as such, the underreach zones of distance relays typically operate in 1 to 1.5 cycles because of the delay caused by the sample window size of the Fourier and the prefiltering algorithm.

On the other hand, distance relays are required to increasingly improve its operation speed, especially for EHV and UHV applications, to maintain power system stability. Faults must be cleared faster than the critical fault clearing time to maintain the transient stability of the system and avoid blackout. The critical fault clearing time is referred as the maximum fault duration for which the system retains stability of operation.

Faster fault clearing can increase the amount of power that can be transferred through the line, also can reduce the stress of the power transformers, improve personnel safety, and avoid equipment damages. As power systems continue to be stretched to capacity, distance relays will be called upon to operate more quickly [1].

With fast developments in the renewable energy, power system source landscape and dynamics are changing as well. Renewable generation appears as a weak source, meaning distance has to deal with a much higher SIRs, which presents a challenge to the existing distance algorithms.

Since full cycle DFT is somewhat slow, which requires a full cycle of samples to estimate the fundamental phasor, naturally phaselet-based algorithms with shorter window size (only use partial sums of the products of the waveform samples and the Fourier coefficients) have been used to improve the phasor estimation speed, such as half-cycle DFT or quarter-cycle DFT. Though the phaselet-based algorithms are faster than the full cycle DFT based algorithms, phasor accuracy is much worse because as the window size is shortened it becomes more difficult to discriminate between the fundamental frequency component and other components. For instance, if the window size is shortened to half cycle, the Fourier algorithm cannot reject even harmonics and DC. As a result, higher transient errors in distance elements can be expected, additional measures must be taken to accommodate such transient errors, such as reduce underreach zone reach, apply more security delays, etc. However, these additional measures may partially or even entirely cancel the initial gain of speed by sample window size reduction on phasor estimation.

In this paper, a new algorithm is presented, in which voltage and current phasors are estimated through 2 short window orthogonal filters with decaying DC accounted so that the adverse impact to phasor accuracy due to DC offset can be minimized. With the application of additional filtering, averaging, switching, and tripping count strategy, both sub-cycle operation time and accuracy (transient overreach less than 5%) for the underreach zones of distance elements can be achieved under various testing conditions, including the variations of CVT types (magnetic VT, passive CVT and active CVT), SIRs, fault types, fault location and fault point on wave.

The rest of the paper is as follows. The short window phasor estimation method and associated testing results are discussed in Section II. CVT transients in conjunction with high SIRs, and its impact to distance element are discussed in Section III. Voltage and current phasors that are used in the sub-cycle distance algorithm, and the calculation methods to obtain these phasors are discussed in section IV. The arming and the overall protection logic of the sub-cycle distance algorithm are discussed in Section V. Section VI evaluates the performance of the sub-cycle distance algorithm. The paper concludes in Section VII.

II. Short Window Phasor Estimation Algorithm

A. Short Window Phasor Estimation with Decaying DC Accounted

It is known that fault currents may contain a decaying DC component due to the point-on-wave at which the fault occurs and the inductive time constant of the system. The short window phasor estimation method used for the sub-cycle distance algorithm begins with setting the decaying DC time constant, which is referred as Ta in this paper. Then poles of fundamental frequency and the decaying DC component are determined using Equations 1, 2, and 3 below [2], where Ts is the sampling period and N is the number of samples per-cycle.

$$\boldsymbol{z_0 = e^{-Ts/Ta}} \quad \textbf{(1)}$$

$$\boldsymbol{z_1 = e^{j\frac{2\pi}{N}}} \quad \textbf{(2)}$$

$$\boldsymbol{z_2 = e^{-j\frac{2\pi}{N}}} \quad \textbf{(3)}$$

Based on the Eular's equation, also with inclusion of the decaying DC component, current signal can be expressed in equation (4) below:

$$\boldsymbol{i(n) = I_D z_0^n + \frac{\dot{I}_P}{2} z_1^n + \frac{\bar{I}_P}{2} \bar{z}_2^n} \quad \textbf{(4)}$$

Where n is the sample index. With 3 or more known current signal samples, the unknown variables ($\boldsymbol{I_D}$, $\boldsymbol{\dot{I}_P}$ and $\boldsymbol{\bar{I}_P}$) can be worked out from equation (5) below:

$$\begin{bmatrix} \boldsymbol{i(W-1)} \\ \boldsymbol{i(W-2)} \\ \dots \dots \\ \boldsymbol{i(1)} \\ \boldsymbol{i(0)} \end{bmatrix} = \begin{bmatrix} \boldsymbol{z_0^{W-1}} & \boldsymbol{\frac{z_1^{W-1}}{2}} & \boldsymbol{\frac{z_2^{W-1}}{2}} \\ \boldsymbol{z_0^{W-2}} & \boldsymbol{\frac{z_1^{W-2}}{2}} & \boldsymbol{\frac{z_2^{W-2}}{2}} \\ \dots & \dots & \dots \\ \boldsymbol{z_0^1} & \boldsymbol{\frac{z_1^1}{2}} & \boldsymbol{\frac{z_2^1}{2}} \\ \boldsymbol{1} & \boldsymbol{1} & \boldsymbol{1} \end{bmatrix} \begin{bmatrix} \boldsymbol{I_D} \\ \boldsymbol{\dot{I}_P} \\ \boldsymbol{\bar{I}_P} \end{bmatrix} \quad \textbf{(5)}$$

Where W is the short window size, which determines the number of samples to be used for the phasor estimation. Use M to denote the W×3 dimensions matrix, I to denote current samples, and X to denote the phasors to be estimated.

$$\boldsymbol{M} = \begin{bmatrix} \boldsymbol{z_0^{W-1}} & \boldsymbol{\frac{z_1^{W-1}}{2}} & \boldsymbol{\frac{z_2^{W-1}}{2}} \\ \boldsymbol{z_0^{W-2}} & \boldsymbol{\frac{z_1^{W-2}}{2}} & \boldsymbol{\frac{z_2^{W-2}}{2}} \\ \dots & \dots & \dots \\ \boldsymbol{z_0^1} & \boldsymbol{\frac{z_1^1}{2}} & \boldsymbol{\frac{z_2^1}{2}} \\ \boldsymbol{1} & \boldsymbol{1} & \boldsymbol{1} \end{bmatrix} \quad \textbf{(6)}$$

$$\boldsymbol{I} = \begin{bmatrix} \boldsymbol{i(W-1)} \\ \boldsymbol{i(W-2)} \\ \dots \dots \\ \boldsymbol{i(1)} \\ \boldsymbol{i(0)} \end{bmatrix} \quad \textbf{(7)}$$

$$\boldsymbol{X} = \begin{bmatrix} \boldsymbol{I_D} \\ \boldsymbol{\dot{I}_P} \\ \boldsymbol{\bar{I}_P} \end{bmatrix} \quad \textbf{(8)}$$

Then phasor matric X can be solved by the equation below,

$$\boldsymbol{X = (M^T M)^{-1} M^T I} \quad \textbf{(9)}$$

where $M^T$is the transposed matrix of M.

It may look like that the computation in the above process is complex, but it is actually simple. The calculation of $(M^T M)^{-1} M^T$ can be carried out off-line because all the elements in M are predetermined. The fundamental phasor $\dot{I}_P$ can be obtained from the convolution operation of the current signal samples with the second row of the predetermined matrix $(M^T M)^{-1} M^T$. The calculation is as simple as the normal convolution.

Let's use H to denote matrix $(M^T M)^{-1} M^T$ as shown in equation (10),

$$\boldsymbol{H = (M^T M)^{-1} M^T} \quad \textbf{(10)}$$

The second row of matrix H can be extracted as a vector of coefficients, h, where the real part and the imaginary part of these coefficients form 2 orthogonal filters, which is shown in Equation (11) below. The vector of coefficients, h, has the same length as the short window length, W.

$$\boldsymbol{h(1:W) = H(2, 1:W)} \quad \textbf{(11)}$$

Once the vector matrix, h, is determined, the fundamental phasor, $\boldsymbol{\dot{I}_P}$(n), can be calculated using Equation (12) presented below, which involves a discrete convolution operation, where i(n) are current signal samples.

$$\boldsymbol{\dot{I}_P(n) = \sum_{k=1}^{W} h(k) i(n-k+1)} \quad \textbf{(12)}$$

B. Short Window Algorithm Performance at Different Time Constant

In the algorithm described above, a time constant, Ta, was preselected to account for the decaying DC component shown in equation (1). However, in a real power system, the time constant for the decaying DC component that is contained in the fault current might be quite different from the value that we preselected, which will depend on the actual X/R ratio of the network at when the fault occurs. As well, the X/R ratio of a network may vary due to network switching or operation mode changes. Below shows the testing results that the short window algorithm with preselected Ta=0.0265s responds to the fault at different time constants (X/R ratios) in comparison with phasors extracted via full cycle DFT and half-cycle DFT respectively.

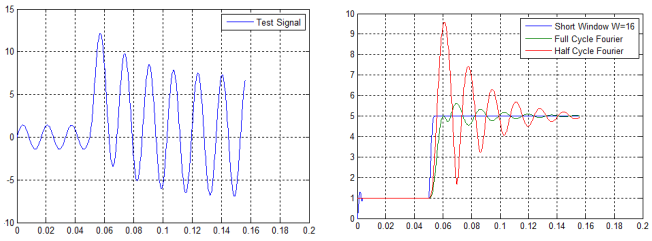

Figure 1. Test signal with X/R=10 (left), fundamental phasor magnitude estimated by short-window, full and half cycle Fourier respectively (right)

The test signal showed in Figure **1** is at X/R=10, which is equivalent to a time constant of 0.0265s in a 60Hz system, exactly the same time constant that we preselected for the sub-cycle distance algorithm. Since the time constant of the test signal and our preselected Ta in the short window algorithm match perfectly, it can be seen that the phasor magnitude estimated by the short window method does not contain any transient errors (oscillations), while the phasor magnitudes estimated by full cycle and half cycle Fourier contain significant transient errors. Besides accuracy, it can also be observed from Figure 1 that the short window method has the fastest response time, which reaches to the final value of the fault current at 6.25ms earlier than the full cycle DFT method and 1.56ms earlier than the half cycle DFT method.

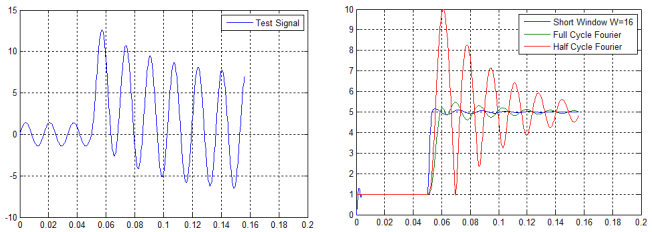

Figure 2. Test signal with X/R=15 (left), fundamental phasor magnitude estimated by short-window, full and half cycle Fourier respectively (right)

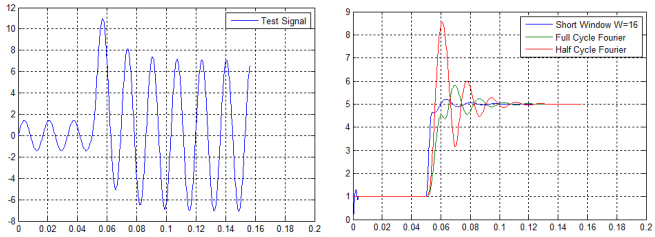

Figure 3. Test signal with X/R=5 (left), fundamental phasor magnitude estimated by short-window, full and half cycle Fourier respectively (right)

The test signals in Figure 2 and Figure 3 are at X/R=15 and X/R=5 respectively, which are quite far from the Ta value (0.0265s) that we preselected for the short window algorithm. However, it can be seen that the phasor magnitude estimated by the short window method still has the best accuracy and fastest response time compared to the full and the half cycle Fourier algorithms.

III. CVT Transients and Mitigation Methods

Besides decaying DC in current signals, which has been accounted in the short window phasor estimation method described in section II. CVT transients in voltage signals in conjunction with high SIRs (System Impedance Ratio) are another factor that can affect distance element performance significantly.

A. CVT Transients vs. CVT Type

Capacitive Voltage Transformers (CVTs) are commonly used as the voltage signal sources for protective relays in HV and EHV systems. Compared to the conventional magnetic VTs, CVTs provide a cost-efficient way for relays to obtain the secondary voltages. However, CVTs also create problems to protective relays. On occurrence of a fault on the line, when the primary voltage collapses, the CVT secondary voltage may not be able to follow its input primary voltage due to the dissipation of the energy that was stored in the stack capacitors and the tuning reactor, which could generate severe transients and can affect the performance of protective relays significantly.

Based on the design of the ferro-resonance suppression circuit, CVTs can be divided into 2 categories, active type and passive type, the former consists of a resistor in series with a parallel LC branch which is tuned to nominal frequency and behaves as an open circuit at nominal frequency; the latter consists of a resistor and a nonlinear inductor which saturates if the voltage exceeds 150% of the nominal secondary voltage [3]. The transients generated from an active CVT are typically severer than that from a passive CVT and is generally more difficult to filter out since it is so close to the fundamental frequency, while the transients from a passive CVT is easier to filter out [5].

Figure **4** and Figure **5** below are 2 examples of transients generated from a passive CVT and an active CVT respectively via simulation. The protected line in the simulation was a short line of 13.36 km, with line impedance of $Z1=0.75\angle 86^0\ \Omega$ secondary. AG fault at the same location was applied in both

situations (Figure 4 and Figure 5), which was at 80% of the line with SIR=30 when Va is at zero crossing. It can be seen that the CVT transients on the fault voltage is much severer in an active CVT than that in a passive CVT, especially in the first 2 cycles after the fault inception.

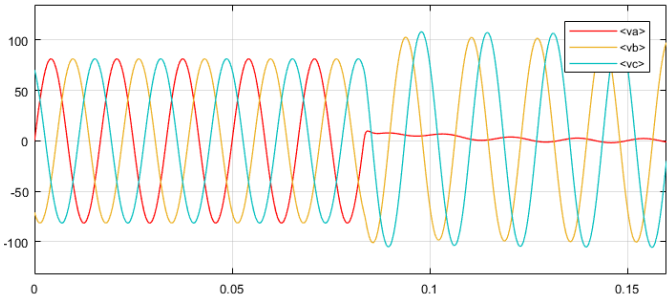

Figure 4. Secondary voltage obtained from a passive CVT with SIR=30

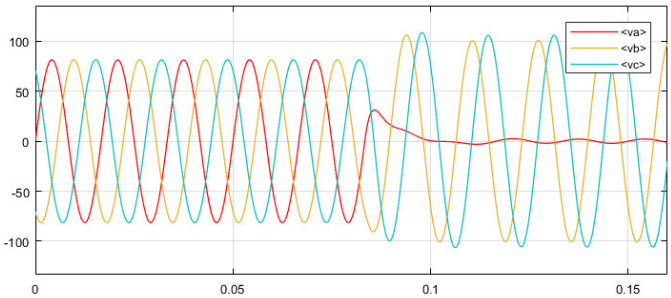

Figure 5. Secondary voltage obtained from an active CVT with SIR=30

B. CVT Transients vs. SIRs

Besides CVT type, fault voltage magnitude level affects the severity of CVT transients as well, the smaller the fault voltage level, the severer the CVT transients. As the SIR increases, the fault voltage level decreases for a fault at a given location. At high SIR, the fault voltage at the reach point can drop to a very small value, which directly affects the distance element measurement accuracy. The CVT transients at SIR=10 is showed in Figure 6 and Figure 7 for the same fault showed earlier in Figure 4 and Figure 5 at SIR=30. It can be seen that the CVT transients at SIR 10 are much less severe than that at SIR 30.

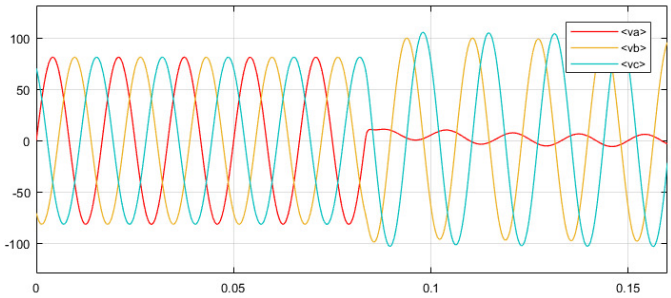

Figure 6. CVT transients at SIR=10 with passive CVT type

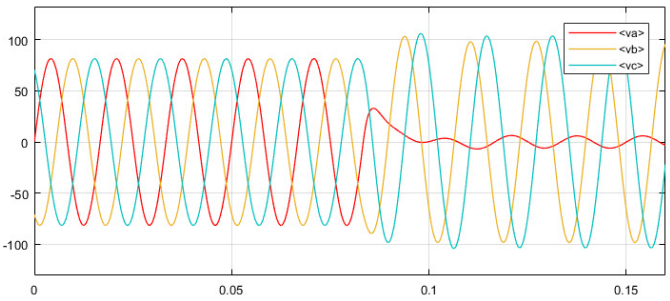

Figure 7. CVT transients at SIR=10 with active CVT type

In addition, voltage point on wave at when the fault occurs also makes a difference on the severity of the CVT transients. The most severe transients are generated when a fault occurs at the zero crossing of the primary voltage, and least severe when the primary voltage at the maximum wave point (+/- 90 degrees). To ensure the security of the sub-cycle distance algorithm, all possible point on wave conditions have been included during our testing.

C. Impact of CVT Transients to Distance Elements

CVT transients can cause problems in distance element and severely affect its performance, in which transient overreach in underreach zones is one of the major issues. For faults located at the reach point, the impedance must be measured accurately in order to ensure the security of the distance element. With CVT transients, however, voltage phasor magnitudes cannot be estimated accurately, which can be over or under-estimated. As shown Figure 8, the phase A voltage magnitude for the same test case listed in Figure 5 is plotted here, it can be seen that after fault inception, phase A voltage magnitude is underestimated initially and then overestimated and then gradually approach to the actual value with both full cycle DFT and half cycle DFT methods. Underestimation of the voltage magnitude translates directly (assuming the current being measured accurately) into the negative error in the measured impedance — a fault would appear to be closer, and result in transient overreach in the underreach zone, where the relay would mis-operate for an external fault.

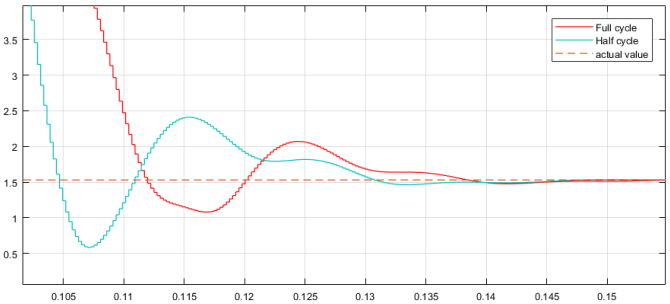

Figure 8. Voltage magnitude estimated via full cycle and half cycle DFT for the same test case of Figure 5

Note that CVT transients may affect the initial pickup of distance overreach zones (zone 2 and above), but since the CVT transient duration is short and the time delays associated with the distance overreach zones are much longer, the mis-

operation on these overreach zones due to CVT transients won't happen.

D. Mitigation Methods

To overcome the transient overreach problem in underreach zones due to CVT transients, several methods have been used [4], including,

- Reach reduction
- Additional delay
- Application of filtering to remove CVT transients
- Combination of above methods based on certain logic, such as SIR detection, CVT transient detection, etc.

Though above methods are all effective to avoid distance transient overreach, however, either protection dependability or operation speed, or both, are compromised with the application of these methods. Among them, filtering techniques to remove or reduce CVT transients have been commonly used by microprocessor relays.

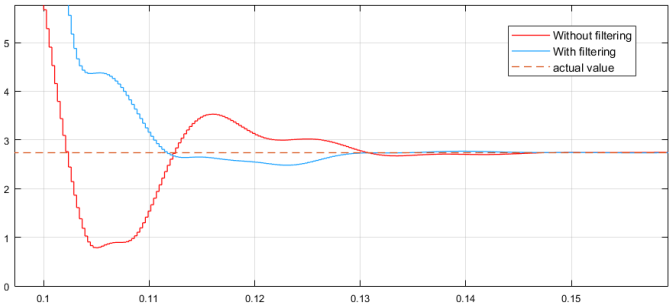

Figure 9. Voltage magnitude estimated via half-cycle DFT with and without prefiltering for active CVT at SIR=20

Paper [3] introduced a method with application of prefiltering, in which CVT transients are effectively removed, however distance element operation speed is affected quite significantly. As shown in Figure **9** above, for a test case with active CVT at SIR=20, the voltage magnitude via half cycle DFT with prefiltering is much more accurate than that without prefiltering, however, with the application of the filtering, it also introduced significant delays (10ms slower for this test case) for the voltage magnitude to approach to the actual value, and it's impossible to achieve sub-cycle distance operation speed with such filtering.

IV. VOLTAGE AND CURRENT PHASORS THAT ARE USED IN THE SUB-CYCLE DISTANCE ALGORITHM

Voltage and current phasors that are used in the sub-cycle distance algorithm are obtained through comprehensive signal processing, including application of different size of filtering, different size of short window phasors via the method described in section II, and the phasors that are calculated via standard Fourier method. More importantly, the final voltage and current phasors are obtained through the combinations of the above-mentioned methods at different stages after fault inception. Note that the decaying DC component contained in the current signal has been effectively removed with the short window phasor estimation method because DC component was accounted in this method, and its impact to distance elements has been minimized. In this section, we will focus more on the voltage signals and how its impact to distance element due to CVT transients is mitigated.

The signal processing in the sub-cycle distance algorithm for obtaining the final voltage and current phasors are shown in Figure **10** and Figure **11** below.

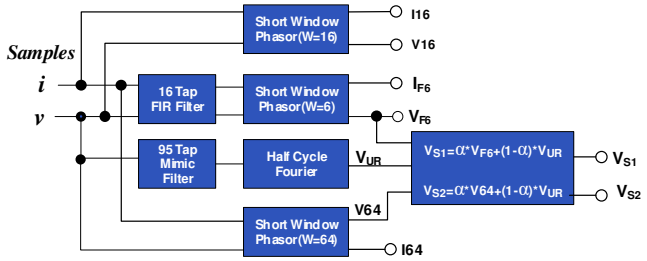

Figure 10. Phasor estimation in sub-cycle distance algorithm (1/2)

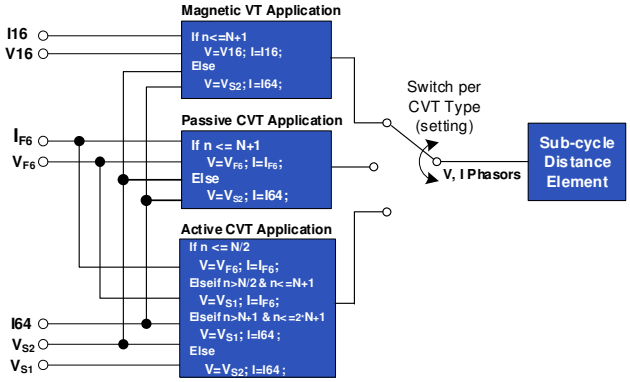

Figure 11. Phasor estimation in sub-cycle distance algorithm (2/2)

Where n is the protection pass count after arming, N is the total number of protection-passes in one cycle (8 in our implementation). V16, I16, V64 and I64 are voltage and current phasors estimated from the short window method (with window size W=16, and W=64 respectively) without prefiltering, V_{F6} and I_{F6} are voltage and current phasors estimated via short window method (with window size W=6) after prefiltering by a16-tap FIR filter, and V_{UR} is the voltage phasor that is calculated via half-cycle DFT after a 95-tap mimic filter filtering (same filtering as introduced in [3]), and α is the weight factor for averaging, and the arming logic will be discussed in next section.

CVT Type showed in Figure **11** is a user setting to indicate what type of CVT (magnetic VT, active CVT or passive CVT) is used to obtain the secondary voltage to the relay for the line protection, which is the only setting required to run the sub-cycle distance algorithm.

The final voltage phasor magnitudes that are obtained per the signal process flow charts (Figure 10 and Figure 11) that are used for sub-cycle algorithm (herein after referred as sub-cycle phasor) are shown below with comparison to the phasor magnitude obtained through long window size mimic filter plus half-cycle DFT per [3], for the same test cases that were listed in Figure **4** and Figure **5** earlier.

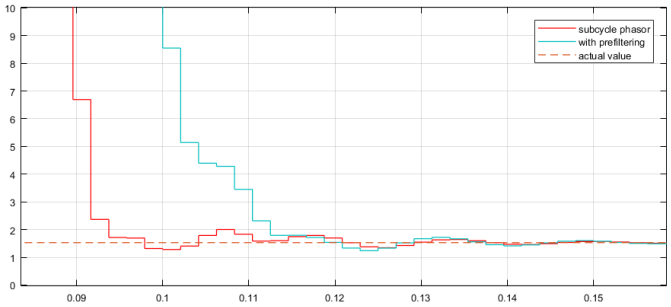

Figure 12. Sub-cycle phasor magnitude and phasor magnitude via prefiltering per [3] for the same test case of Figure 4 with passive CVT at SIR=30

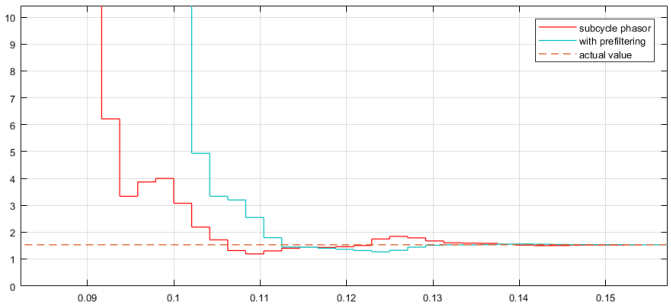

Figure 13. Sub-cycle phasor magnitude and phasor magnitude via prefiltering per [3] for the same test case of Figure 5 with active CVT at SIR=30

From Figure 12 and Figure 13, it can be seen that the phasor magnitudes that are obtained for sub-cycle algorithm and the phasor magnitudes that are obtained via long window size prefiltering have the same or similar accuracy in terms of the underestimation of voltage magnitudes. However, sub-cycle phasor magnitudes approach to the voltage actual value much faster. For the 2 test cases we showed above, it's 18.7ms earlier for passive CVT at SIR=30, and 8.25ms earlier for active CVT at SIR=30. Note that, as discussed earlier, CVT transients caused by an active CVT are difficult to be filtered out. In the sub-cycle distance algorithm, we also use weighted average with the phasors obtained from the long window size prefiltering to further mitigate the CVT transients for active CVT type applications, as a result, the response time for active CVT is significantly slower than that for passive CVT, especially at higher SIR.

The impedance trajectories for test case of Figure 5 based on the voltage phasors obtained by full cycle Fourie without prefiltering, and based on the voltage phasors obtained by half-cycle DFT plus long window size prefiltering, and based on phasors obtained per sub-cycle signal processing (sub-cycle phasor) are shown in Figure 14, Figure 15 and Figure 16 respectively, where decaying DC components in current signals have been filtered out either by the mimic filter or by the short window method with decaying DC accounted.

It can be seen from Figure 14 that severe (67%) transient overreach would happen if the voltage phasors were obtained by full cycle Fourie without prefiltering.

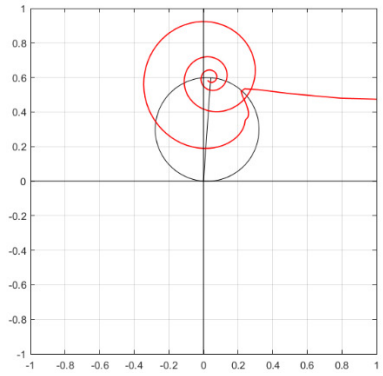

Figure 14. Impedance trajectory based on voltage phasors that are obtained by full cycle Fourie without prefiltering

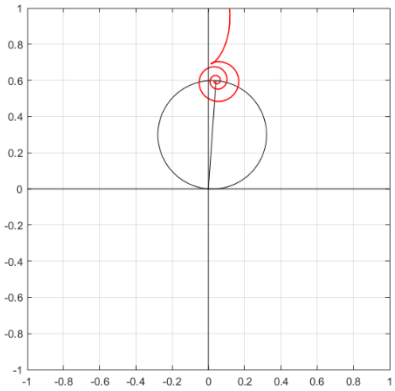

Figure 15. Impedance trajectory based on the voltage phasors obtained by half-cycle DFT plus long window size prefiltering

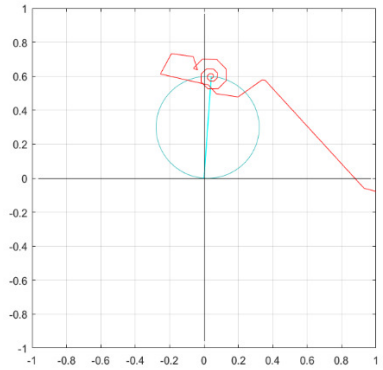

Figure 16. Impedance trajectory based on the sub-cycle phasors

In comparison， the severity of transient overreach has been greatly reduced in both voltage phasors obtained by half-cycle DFT plus long window size prefiltering and phasors obtained per sub-cycle signal processing charts (sub-cycle phasors). The transient overreach has been reduced from 67% (Figure 14) to 16% (Figure 15 and Figure 16). However, this reduction is still not enough to make the transient overreach be less than 5%. Additional measures need to be taken to further reduce transient overreach as well as ensure security and selectivity of the distance protection algorithm.

A. *Tripping Count Strategy*

In [3], a double zone (inner and outer) solution has been implemented to reduce the underreach zone transient overreach further, in which the inner zone has its reach dynamically adjusted based on the voltage magnitude from 80% of the set reach for the SIR of 30, up to 95% for the SIR of 0.1, and outer zone has its reach fixed at 100% of the set reach. No extra delay is applied for inner zone, but some extra delay is applied for outer zone to prevent maloperation.

In the sub-cycle distance algorithm, further improvements have been made, where the distance underreach zone is divided into several areas as shown in Figure 17 below, referred as tripping count strategy, the tripping decision will be made based on an accumulated count depending on where (in which divided areas) the impedance trajectory falls into. Depending on the impedance trajectory, different count increment is applied. If falling into the green area (lemon shape area or the small circle near origin), fast increment is applied; if falling into the yellow area (90% of the original Mho), medium increment is applied; if falling into the pink area-1 (at 10% inside of original Mho), slow increment is applied; if in the pink area-2 (at 10% outside of the original Mho), negative slow count is applied; if outside the pink area and outside the circle near the origin, or directional element fails to pick up, negative fast count is applied. Also, the trip decision is supervised by other comparators, including directional, phase selection, OC, etc.

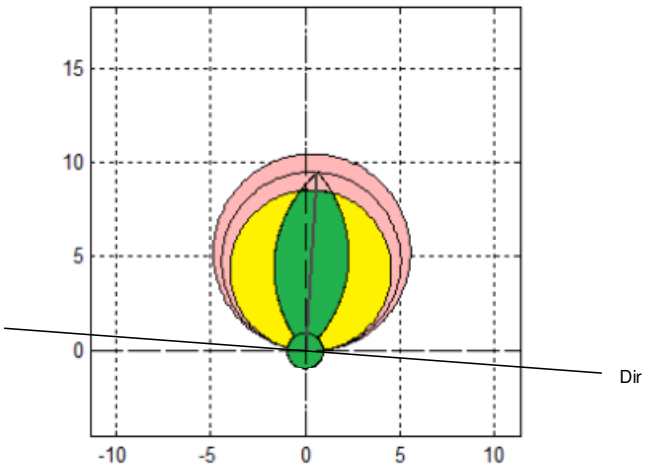

Figure 17. Tripping count strategy

Similar tripping count strategy is applied to quadrilateral characteristic.

B. *Incremental Quantities-based Phase Selection*

To ensure selectivity and security of the sub-cycle distance algorithm, phase selection supervision is applied. Since the sub-cycle distance algorithm only runs for very short time (3 cycles), incremental quantities-based phase selection algorithm is a perfect solution, which can identify fault type correctly and quickly. Also, if the fault is evolved into a different type during this 3-cycle window, new fault type shall be automatically recognized. In our design, incremental phase to phase current quantities (present phasor minus the phasor at 3 cycles before) have been used for this purpose. Based on the relations among three incremental phase to phase current quantities (ΔI_{AB}, ΔI_{BC}, and ΔI_{CA}), fault type can be identified as shown in the table below [6], in which the magnitudes of the three phase-to-phase superimposed currents are compared against a threshold to determine the fault loop.

Ph-Ph Delta I / Loop selected	A	B	C	AB	BC	CA
ΔI AB Valid	yes	yes	no	yes	no	no
ΔI BC Valid	no	yes	yes	no	yes	no
ΔI CA Valid	yes	no	yes	no	no	yes

V. Arming and Overall Protection Logic

A. *Arming*

For implementation simplicity and efficiency, as well as for protection dependability, the sub-cycle distance algorithm only acts as an accelerator and a complement to the regular phasor-based distance element. In our design, the sub-cycle distance algorithm runs only for 3 cycles after it is armed, and then exits itself. During this 3-cycle window, the sub-cycle algorithm runs in parallel with the existing regular phasor-based distance element as shown in Figure **18**, each can independently activate the distance pickup operand.

The regular phasor-based distance element always runs regardless of the status of the sub-cycle distance algorithm. With this manner, only speed and security are critical factors to the sub-cycle distance algorithm, but not the dependability because the regular phasor-based distance element can be relied on to clear the fault in case the sub-cycle distance algorithm fails to pick up. Even though there is no stringent requirement on dependability, however per our testing, the sub-cycle distance algorithm is also dependable. For faults at 90% of reach or below with all the severe transient conditions, it operated 100%.

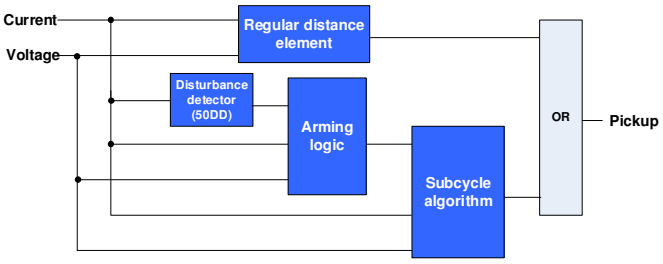

Figure 18. Sub-cycle distance integration with regular distance element

The arming logic of the sub-cycle distance algorithm is shown in Figure 19, which is armed through a fault detector 50DD as shown in Figure 20, where I_1, I_2, I_0 are positive, negative and zero sequency currents, and I_1', I_2', I_0' are the positive, negative and zero sequency currents at 2 cycle before.

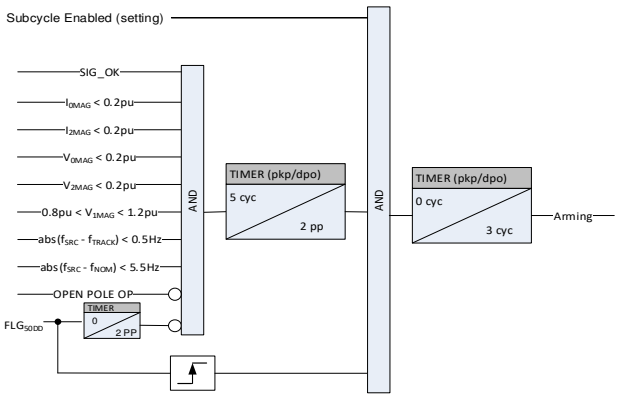

Figure 19. Sub-cycle distance algorithm arming logic

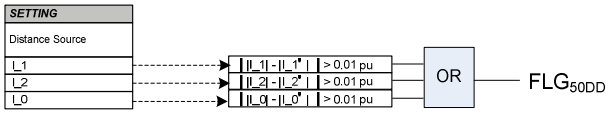

Figure 20. Fault detector 50DD

Once it is armed, the timer with 3 cycle dropout delay opens a 3-cycle window to allow the sub-cycle algorithm to run. When this window expires, it can be armed again only after the system returns to "normal" and stays "normal" for 5 consecutive cycles.

Such normal conditions are defined as:

- Zero-sequence current is less than 0.2 pu
- Negative-sequence current is less than 0.2 pu
- Zero-sequence voltage is less than 0.2 pu
- Negative-sequence voltage is less than 0.2 pu
- Positive-sequence voltage is between 0.8 and 1.2 pu
- Source frequency differs from tracking frequency by less than 0.5 Hz
- Source frequency differs from nominal frequency by less than 5.5 Hz
- No open pole condition exists
- SIG_OK is validated for signal quality

VI. Performance Evaluations

The sub-cycle distance algorithm was thoroughly tested, including playback testing of more than 5000 Comtrade cases, and 3rd party acceptance testing via RTDS dynamic simulation.

A. Playback Testing of Comtrade Cases

More than 5000 Comtrade cases were generated through EMTP and Matlab simulations and saved as Comtrade format with the following variations:

- VT Type (0,1,2,3,4)
- SIR Values (0.1, 1.0, 10, 20, 30, 60)
- Fault Type (AG, AB, ABC)
- Fault Location (0%, 20%, 40%,60%, 70%, 80% 90%,105% of reach)
- POW (0^0, 30^0, 60^0, 90^0, 120^0, 150^0, 180^0)

Total number of test cases 5x6x3x8x7=5040 cases.

Note that the fault location at 105% of reach is purposely used to check the transient overreach of the distance element, where the underreach zone must not operate at this location to ensure transient overreach won't exceed the 5% limit. 5 different VTs were simulated and tested, including 1 magnetic VT type, 1 active CVT type, and 3 different passive CVTs.

The sub-cycle distance algorithm passed all the test with the playback of these Comtrade cases and stayed secure for fault location at 105% of reach. The operation time with different POW at these locations were averaged and plotted for phase distance and ground distance respectively.

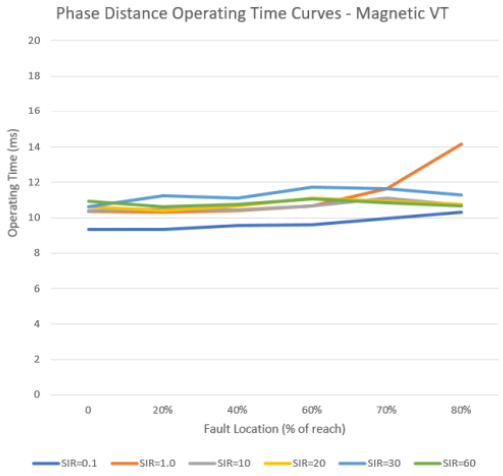

Figure 21. Phase distance operating time curves – Magnetic VT

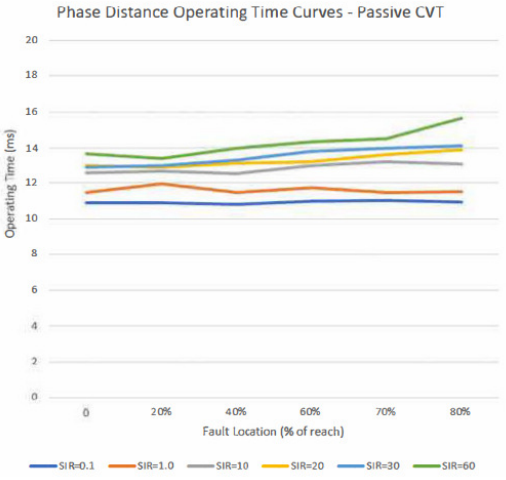

Figure 22. Phase distance operating time curves – passive CVT

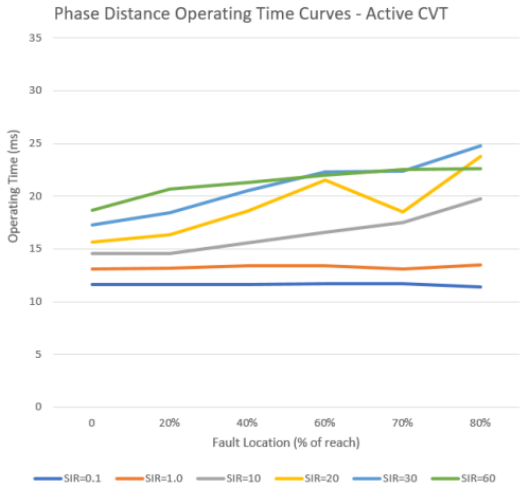

Figure 23. Phase distance operating time curves – active CVT

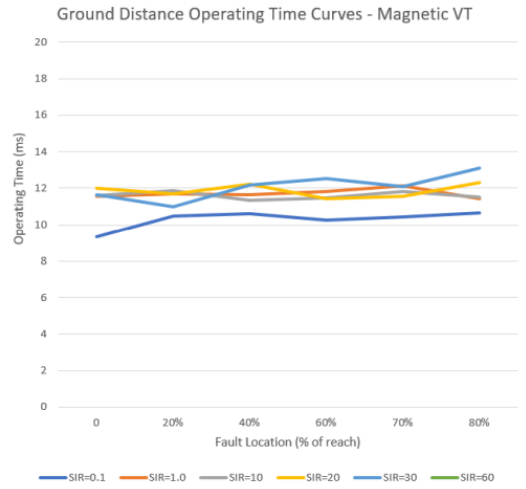

Figure 24. Ground distance operating time curves – Magnetic VT

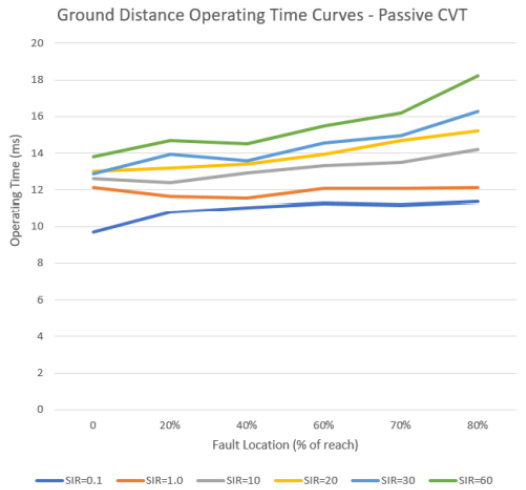

Figure 25. Ground distance operating time curves – passive CVT

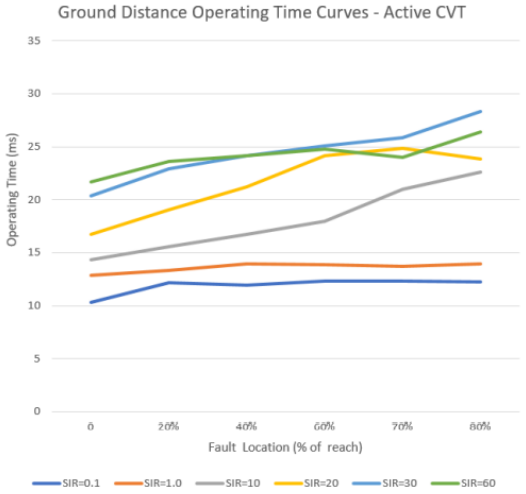

Figure 26.Ground distance operating time curves – active CVT

From the operating time curves in above plots, it can be seen that the sub-cycle distance algorithm works well for magnetic VT and passive CVT, which operates in less than a power cycle for SIR up to 60. However, for active CVTs, the operating time is sub-cycle only at lower SIR (SIR<5).

B. Third Party Acceptance Test

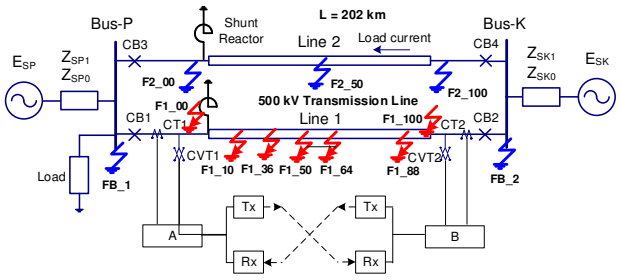

Figure 27. RTDS Power System Model

Besides the playback testing of the over 5000 Comtrade cases, third party acceptance test via RTDS dynamic simulation was also carried out to confirm the performance of the sub-cycle distance algorithm. The RTDS power system model used for this testing is shown in Figure 27 above, in which several hundreds of cases were simulated and tested.

It's required that the relay trip in less than a power cycle for all the internal faults and stay secure for all external faults. Test cases included 4 fault types (AG, AB, ABG, ABC) and 2 POW (0^0, 90^0), with single line and double line configuration variations, and also involved CT saturation, current reversal, evolving faults, switch on to fault, frequency variations, application of different pilot schemes (POTT, PUTT, DCB).

The relay with the sub-cycle distance accelerator algorithm passed all the test, which operated in less than a power cycle for all the internal faults tested and stayed secure for all external faults tested at various testing conditions mentioned above.

VII. Conclusions

The following points summarize the sub-cycle distance algorithm we presented in the paper:

- In this paper, a short window-based phasor estimation algorithm with decaying DC accounted has been developed to achieve distance sub-cycle operation time, in which CVT type is the only setting needed to run this algorithm.
- The sub-cycle distance algorithm only acts as an accelerator and a complement to the regular full cycle Fourier phasor-based distance element. In our design, the sub-cycle distance algorithm only runs for 3 cycles upon it is armed, and then exits itself.
- During the 3-cycle arming window, the sub-cycle distance algorithm is ORed with the regular phasor-based distance element, therefore the dependability of the overall distance protection won't be affected at all.
- The short window phasor estimation method removed decaying DC and CVT transients effectively, also with additional filtering, averaging, switching, and tripping count strategy that are implemented in the sub-cycle distance algorithm, the overall distance protection is secure. Based on testing, the underreach zone transient overreach is less than 5% for SIR up to 60 with either magnetic VTs or CVTs.
- With the sub-cycle distance algorithm enabled, the average operating time is less than 1 power cycle for faults at 80% of reach or below at all SIRs tested (0 to 60) for magnetic VT and passive CVTs, and at SIR<5 for active CVTs.
- Though there's no stringent requirement to the sub-cycle distance algorithm in terms of dependability because of the OR-Gate used with the regular distance algorithm, the sub-cycle distance algorithm itself is dependable as well. Based on testing, it operated 100% for faults at 90% of reach under very severe testing conditions, including very weak sources (SIR=60) with severe CVT transients and decaying DC.

VIII. References

[1] Dale Finney, Zhiying Zhang, Jorge Cardenas, "Ultra-Fast Distance Protection", 10th IET International Conference on Developments in Power System Protection *(*DPSP 2010), Manchester, UK

[2] Hengxu Ha, Zhiying Zhang, "Systems and Methods to Improve Distance Protection in Transmission Lines", patent publication 20210096166

[3] Bogdan Kasztenny, Dave Sharples, Vince Asaro, Marzio Pozzuoli, "Digital Relays and Capacitive Voltage Transformers: Balancing Speed and Transient Overreach", Georgia Tech Protective Relay Conference, 2000, Atlanta, USA

[4] Venkatesh C, Zhiying Zhang, "CVT Transients – Causes, Effects and Solutions", WPRC, Oct. 2019, Spokane, USA

[5] Roger A. Hedding, "CCVT Transients Fundamentals", 65th Annual Conference for Protective Relay Engineers, 2012, College Station, Taxes, USA

[6] P Horton, S Swain, "Using Superimposed Principles (Delta) in Protection Techniques in an increasingly Challenging Power Network", 70th Annual Conference for Protective Relay (CPRE), 2017, College Station, Taxes, USA

[7] GE publication 1601-0089-AM1, "D60 Line Distance Protection System", 2022.

IX. Biographies

Zhiying Zhang received his B.Sc and M.Sc. degrees from the North China Institute of Electric Power (now North China Electric Power University) and a Ph.D. degree from the University of Manitoba, Canada, all in Electrical Engineering. He has over 35 years of working experience with electric utilities and with relay manufactures in various technical positions. Since 2007 he has been with General Electric, and currently holds the position of principal application engineer at GE Grid Solutions in Markham, Ontario. Zhiying is a registered professional engineer in the province of Ontario, and a senior member of IEEE.

Ilia Voloh received the Electrical Engineering degree from Ivanovo State Power University, Ivanovo, Russia. He is currently a Senior Applications Consultant with GE Grid Solutions, Markham, ON, Canada. He has authored and coauthored more than 60 papers presented at the major North America Protective Relaying conferences. His areas of interest are advanced power system protection algorithms and advanced communications for protective relaying. He is a member of IEC TC95 and TC38 committees, member of CIGRE SC B5, senior member of the IEEE and an active member of the main IEEE PSRC committee.

Hengxu Ha obtained his PhD degree of electrical engineering in Xi'an jiaotong university (China) in April 2003, Master of Science degree from Shandong university in March 1999, and Bachler degree from Three Gorge university in July 1993. He experienced in research works on power system automation, control and protection for almost 30 years. He is now an emerging technologies manager in GE grid solutions, Stafford, UK. Till now he has got 28 patents filed and published, in which 23 of them have been granted.

Zhiwu Fu received his Bachelor and Master degrees from the Central South University in China. He has over 16 years of working experience with protective relay development. Since 2009 he has been with General Electric, and currently holds the position of Senior Software Engineer at GE Grid Solution in Stafford, UK.