Compensation of impedance measurement error due to arcing

J. Blumschein*, C. Dzienis[+]

** Siemens AG, Smart Infrastructure Division*
[+]University of Applied Sciences Zittau/Görlitz

Keywords: Distance Protection, Fault Location, Impedance Calculation, Arcing

Abstract

Arcing is a phenomenon which is closely related to short circuits in electrical systems. The nature of arcing can be different but, in any case, there is no universal mathematical model to describe arcing. In a general approach arcing is described with a non-linear, but only resistive voltage-current characteristic.
Based on this assumption the distance protection is using the R-reach of the characteristic to cover the arc impedance. For the impedance-based fault location a similar approach applies. If the arc is only resistive, the reactance measurement used for the fault location is not influenced.
This paper presents two real cases where impedance measurement errors due to arcing can heavily influence the behaviour of distance protection and impedance-based fault location.
In the first example the fault locator estimates a location with an unacceptable measurement error. This happens after a successful trip of the line differential protection on a 400kV line with single side infeed only. The arcing impacts the voltage measurement in magnitude and phase angle which finally leads to the incorrect estimation of the fault location.
The second example is about distance protection applied to a medium voltage cable. Due to the arcing a fault in zone 1 is measured to be outside of zone 1 for a long time. After approximately 170 ms the characteristic of the arc is changing which enables the distance protection to measure the fault in zone 1 and send a trip command to clear the fault.
The paper analyses the two cases in detail and suggests a method how to improve the impedance measurement for distance protection and fault location in such cases of arcing.

1 Introduction

Distance protection is used worldwide to protect the lines for the transmission and distribution of electrical energy against consequences of electrical faults. The distance protection must detect these faults and initiate a trip command to isolate the faulted line.
If a fault is isolated by tripping the faulted line, a fault locator is used to calculate the exact location of the fault. Both, distance protection and impedance-based fault locator determines the fault impedance $\underline{Z}_F$ from the voltage $\underline{U}_A$ and the current $\underline{I}_A$ measured at the relay location like shown in figure 1 according to Ohm's law:

$$\underline{Z}_F = \frac{\underline{U}_A}{\underline{I}_A} \qquad (1)$$

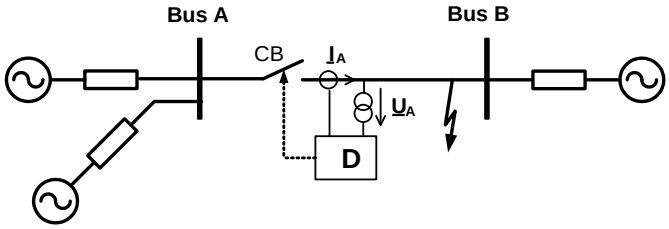

Figure 1: Basic principle of distance protection

A common method widely used for distance protection and fault location is to calculate the impedance according to equation (1) based on voltage and current phasors. Typical methods to estimate the phasors of voltages and currents are based on Discrete Fourier Transform (DFT), Fast Fourier Transform (FFT) or similar algorithm.
The real part Re($\underline{U}_k$) and the imaginary part Im($\underline{U}_k$) of the voltage phasor can be calculated from the individual voltage samples according to formula (2) and (3).

$$Re(\underline{U}_k) = \sum_{n=0}^{N-1} (u_{k-n} \cdot cos(2\pi \cdot f_r \cdot n \cdot T_A)) \qquad (2)$$

$$Im(\underline{U}_k) = \sum_{n=0}^{N-1} (u_{k-n} \cdot \sin(2\pi \cdot f_r \cdot n \cdot T_A)) \qquad (3)$$

u_{k-n}	- Individual voltage sample
k	- current voltage / voltage sample
n	- index
f_r	- rated frequency (for instance 50 Hz or 60 Hz)
T_A	- sampling interval (time between two samples)
N	- number of samples per period

In this case the voltage phasor $\underline{U}_k$ represents the fundamental component of the voltage signal because the individual voltage samples are filtered using a cosinus and sinus function of the rated frequency.
In general, this voltage phasor should represent the driving voltage of the system at relay location. The filtering is used to attenuate noise and other disturbance in the voltage signal.
For the estimation of the current phasor the same approach is used.

2 First example: Wrong fault location due to arcing

The first example is about an unacceptable measurement error of the fault locator for a single-phase to ground fault on a 400kV line. This happens after a successful trip of the line differential protection. Figure 2 shows the single line diagram. The line was fed from the local end only because the remote end was open at the time of fault inception.

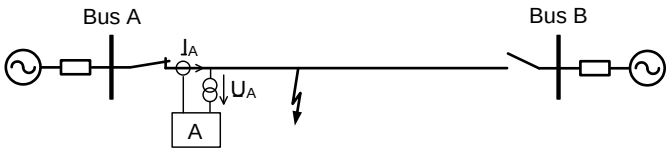

Figure 2: Single line diagram for the fault on the 400 kV line with remote end open

Normally in such situation with local infeed only the impedance-based fault locator can obtain a fault location with high accuracy. In this case the deviation of the fault location given by the relay A was greater than 100%. An offline fault location based on the fault record obtained by relay A confirmed the fault location estimated by the relay.

Figure 3 illustrates the fault impedance in the complex plane. The small red squares are indicating the impedances for each measurement point. It can be seen that the impedance is measured to be in zone 1 quite closed to the R-reach of zone 1.

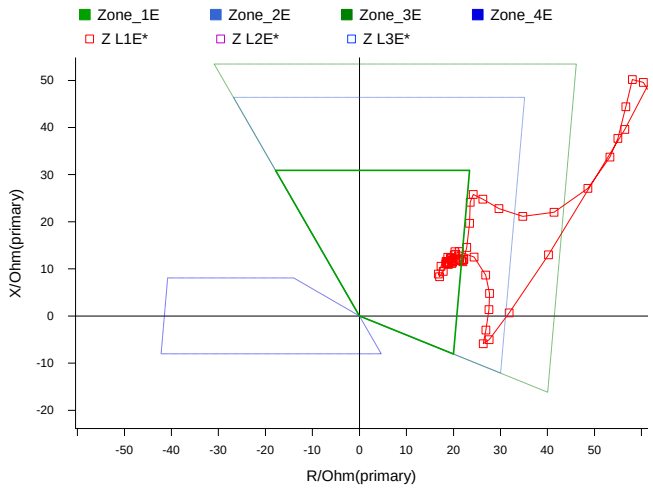

Figure 3: Location of the fault impedance in the complex plane

Figure 4 shows the currents and voltages for this fault in phase A. The current of phase A is already rising before fault inception but after fault inception the current is quite stable in magnitude and phase and looks quite sinusoidal.
The voltage of phase A does not have a stable state during the duration of the fault which could be a problem for the impedance measurement needed for the fault location.

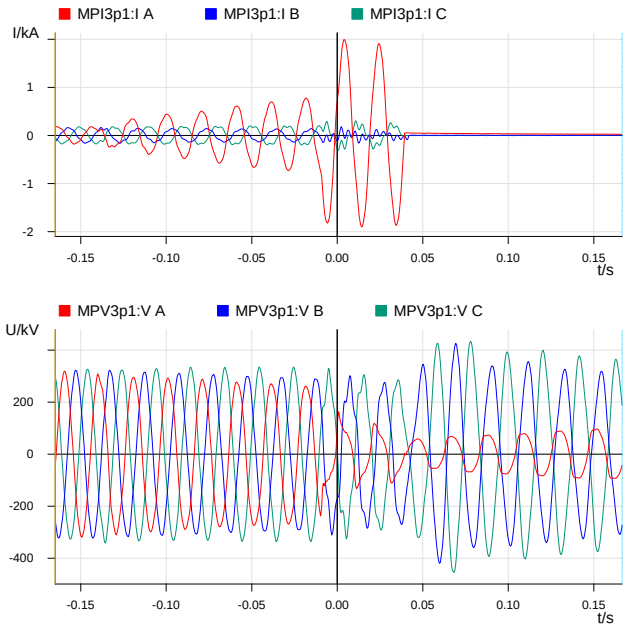

Figure 4: Currents and voltages of the phase-A to ground fault

Figure 5 shows the voltages in more detail. The voltage of the faulted phase A has a shape which is typical for a special kind of arcing. After zero crossing the voltage is rising fast quite similar like before fault inception. After a short time if the voltage reaches a critical limit, the arcing starts and breaks down the voltage to a lower level. Based on this lower level the voltage reaches the next zero crossing.

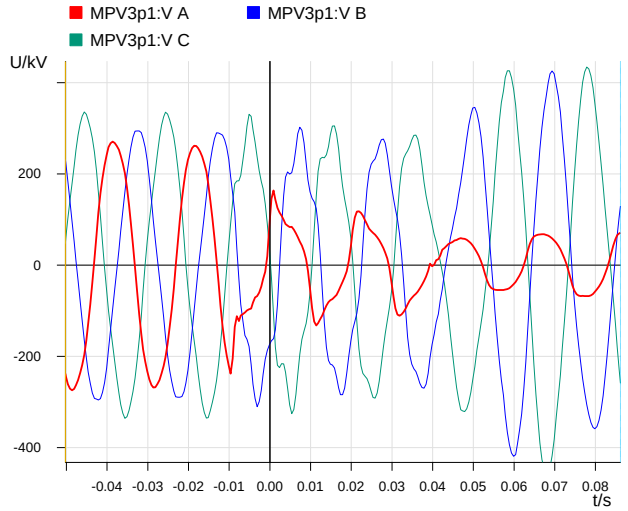

Figure 5: Voltage signal of the phase A to ground fault

This arcing impacts the voltage measurement in magnitude and phase angle which finally leads to the incorrect estimation of the fault location.

3 Second example: Delayed trip of distance protection due to arcing

The second example describes the behaviour of the distance protection applied to a medium voltage cable system. Figure 6 shows the single line diagram including the grading of the zones for the distance protection D1. The first zone Z1 for instantaneous trip of distance protection is set as usual to 80% of the protected line. Z2 and Z3 are used for backup protection for faults on the adjacent lines.

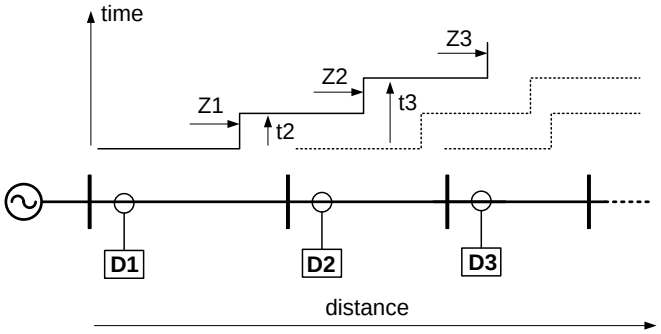

Figure 6: Single line diagram for a distribution feeder including zones of distance protection

Figure 7 shows currents, voltages, and binary signals for a fault in zone 1 of the distance protection D1 according to figure 6. Similar to the example presented in chapter 2, the current of the faulted phase is quite stable in magnitude and phase and looks quite sinusoidal too. The voltage of the faulted phase starts at fault inception with the typical shape of unstable arcing. After approximately 170 ms the effect of unstable arcing disappears, at least for the positive half of the sinus wave. At the same time the distance protection measures the fault impedance located in zone 1 and issues a trip command.

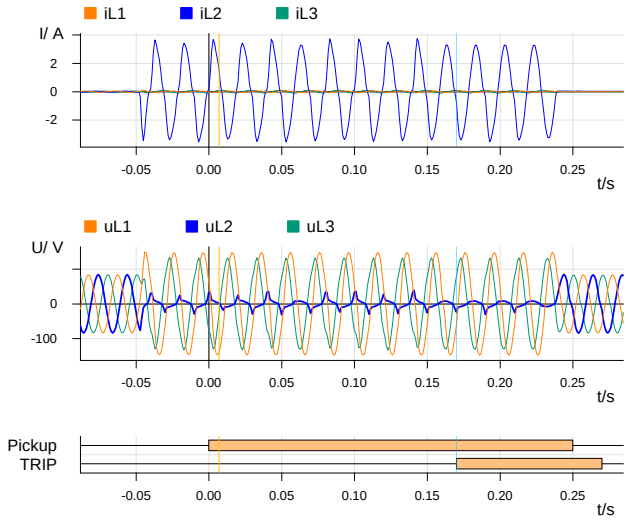

Figure 7: Currents, voltages, and binary signals for the fault in Zone Z1

Figure 8 shows the location of the fault impedance in the complex plane. The yellow cursor marks the fault impedance at the time of fault inception according to the yellow cursor in figure 7. At this time the impedance is measured inside zone 2 and zone 3 but outside zone 1 of the distance protection. For that reason, the distance protection issues a pickup but no trip signal as shown in figure 7.
The blue cursor marks the measured impedance approximately 170 ms later according to the blue cursor in figure 7. At this time the impedance is measured in zone 1 which leads to an instantaneous trip command of the distance protection.

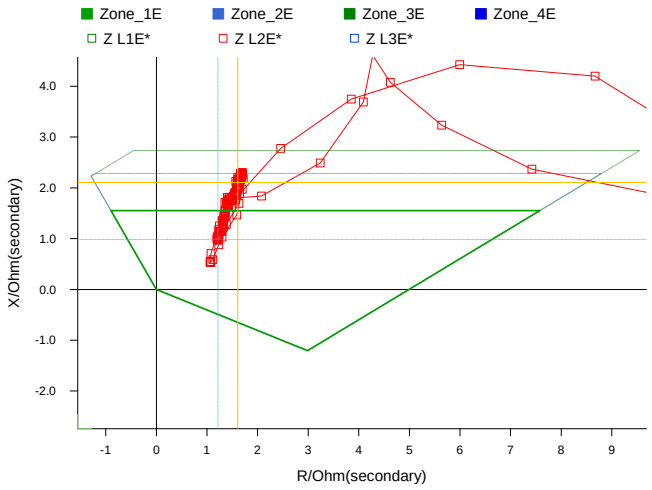

Figure 8: Location of the fault impedance in the complex plane at fault inception and tripping

Figure 9 shows the phasors of currents and voltages at fault inception and tripping. Theses phasors are the basis for the calculation of the fault impedances shown in figure 8. The voltage at fault inception shown in the left diagram has a magnitude and phase shift much greater than the voltage at the time of tripping which is shown in the right diagram.

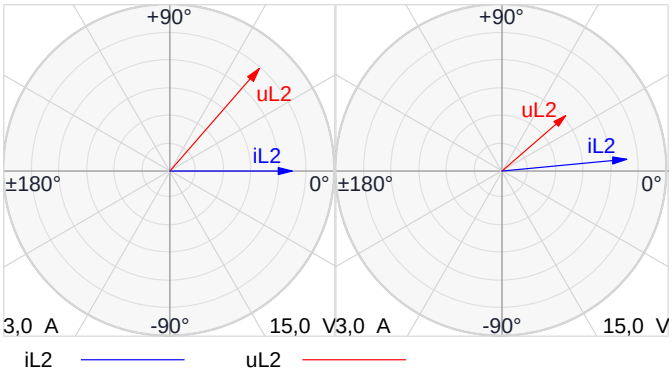

Figure 9: Current- and voltage-phasors at fault inception and tripping

4 Wrong estimation of voltage phasor due to unstable arcing

As already explained in chapter 2 and chapter 3 the wrong estimation of the voltage phasor due to the re-arcing is the main reason for the wrong estimation of the fault impedance. This leads to a wrong result of the fault locator or a delayed tripping of the distance protection.
Figure 10 gives a graphical illustration of the problem. The blue marked signal "*K1: uL1 A*" represents the original voltage signal including the non-linear behavior of arcing especially in each first part of each half-wave.
The red marked signal "*K2: uL1 A*" represents a voltage signal which is re-calculated from the phasor estimated from the blue marked original signal "*K1: uL1 A*".

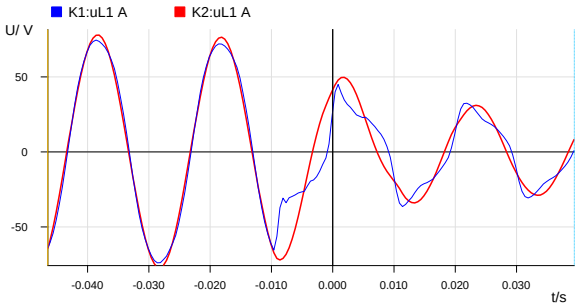

Figure 10: voltage signal, recalculated from the phasor estimation applied to an original voltage signal disturbed by arcing

In other words, the red marked signal "*K2: uL1 A*" in figure 10 represents the fundamental component of the of the blue marked original signal "*K1: uL1 A*" based on a Fourier analysis. The great deviation in phase and magnitude between both signals is related to the great amount of harmonics in the original Signal "*K1: uL1 A*" as shown in figure 11.

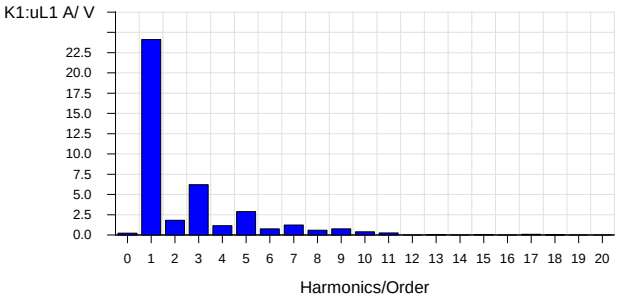

Figure 11: Harmonic content of the voltage signal disturbed by arcing

As shown in figure 11 the third, fifth and seventh harmonics are dominant in the spectrum of the voltage disturbed by the arcing spikes.
Unfortunately, in this case the voltage phasor based on the fundamental component of the voltage and calculated by a Fourier analysis is not a good representation of the voltage of the faulted phase at relay location.

5 Compensation of impedance measurement error

Based on the results of the analysis, given in the previous chapter a correction of the impedance measurement error is possible. Therefore, a structure like shown in figure 12 is suggested.

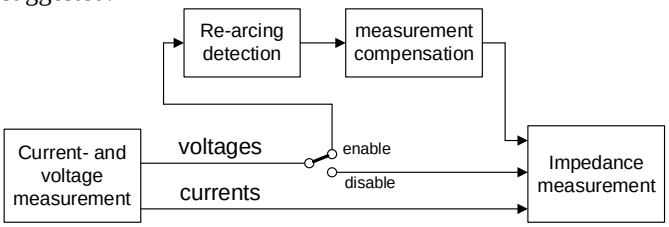

Figure 12: Block diagram of the suggested impedance measurement compensation

In a first step the voltage signals are analysed for disturbances due to re-arcing. This can be done in time domain based on the different shape of the signal for the first and the second half of each half-wave or in frequency domain analysing the content of harmonics in the voltage signal.
If a re-arcing is detected in the faulted voltage the correction of the voltage signal can be done using the following two main criteria explained in time domain:

1. The corrected voltage signal should have the same zero crossings compared to the original signal
2. The corrected voltage signal should follow the shape of the second half-wave of the original signal as precise as possible

Figure 13 shows the result of this compensation for the re-arcing voltage in the time domain. The blue marked signal "*K1: uL2 B*" is the original re-arcing voltage from the example presented in chapter 3. The red marked signal "*K2: uL2 B*" is the corrected voltage, compensated according to the criteria above. Both signals are identical if the original signal follows a pure sinusoidal shape. The correction algorithm only removes the spikes in the voltage signal which are originating from the re-arcing.

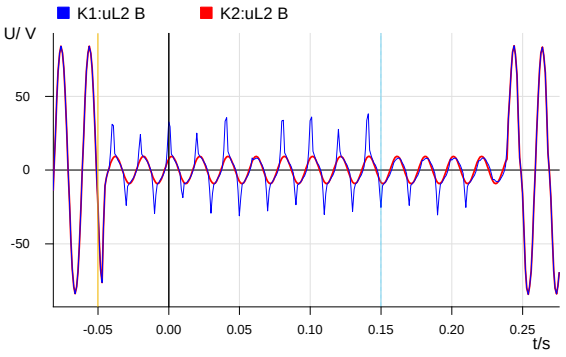

Figure 13: Re-arcing voltage signal before and after correction

Figure 14 shows the result of this compensation for the re-arcing voltage in the phasor diagram. The blue marked signal "*K1: uL2 B*" is the original re-arcing voltage phasor from the example presented in chapter 3. The red marked signal "*K2: uL2 B*" is the corrected voltage phasor, compensated according to the criteria explained above.
The left diagram shows the original voltage phasor and the compensated voltage phasor at fault inception. The difference between both phasors is much greater compared to the right diagram which shows the phasors at the time of tripping. This is because according to figure 13 the re-arcing happens at both half-waves at fault inception but only at the negative half-wave at the time of tripping.

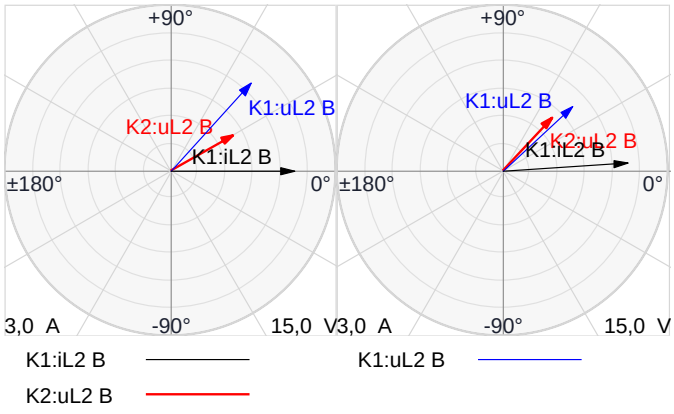

Figure 14: Re-arcing voltage phasor, before and after correction

Figure 15 shows the location of the corrected impedance in the complex plane. Different to the trajectory of the impedance measured with the original voltage as shown in figure 8, the impedance based on the compensated voltage is measured to be in Zone one just from the beginning of the fault.

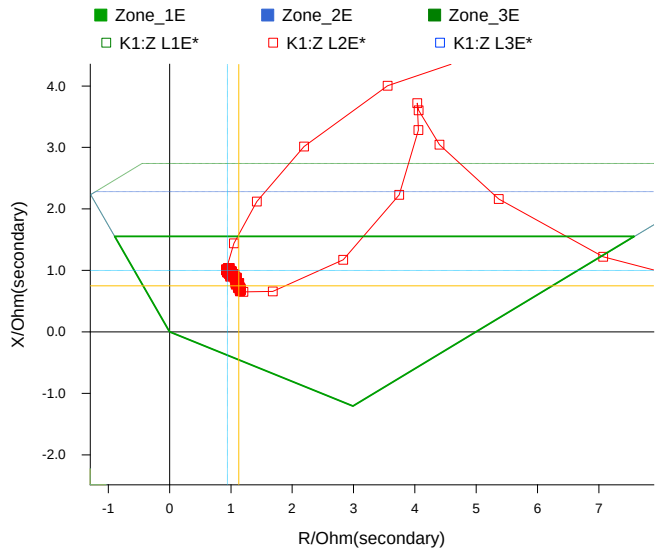

Figure 15: Location of the fault in the complex plane after voltage correction

6 Conclusion

Using two real world examples it was explained how arcing can impact the impedance measurement of distance protection and fault locator. A main reason was identified related to phasor estimation algorithms based on DFT.
Based on these results a compensation was suggested which can be applied to correct the significant measurement error.

7 References

1. Dr. Rainer Krebs, Verfahren und Einrichtung zur Signalkorrektur, Offenlegungsschrift DE 42 30 649 A1, 17.03.1994
2. Robert Fenkl, Hagen Grünert, "Mittelspannungsnetz-strukturen, Schutztechnik und Smart Grids", etz, Heft 10/2012
3. G. Ziegler, "Numerical Distance Protection: Principles and Application", Siemens Aktiengesellschaft, 4th Edition, ISBN 978-3-89578-381-4, 2011.
4. Manual SIPROTEC 5 Distance Protection, Line Differential Protection, and Breaker Management for 1-Pole and 3-Pole Tripping 7SA87, 7SD87, 7SL87, 7VK87, Version V6.00 and higher, SIEMENS AG, C53000-G5040-C011-6

8 Biographies

Jörg Blumschein studied technical cybernetics and process measurement at the University Magdeburg where he became a graduated engineer in 1992. Since 1992 he works with SIEMENS in the development department of protection relays. Today he is the Principal Key Expert for Protection.

Cezary Dzienis graduated with a degree in Electrical Engineering from Warsaw University of Technology in 2003. He then worked for university's Division of Industrial Electronics and Control System until 2004. Since then, he worked for Chair of Electric Power Networks and Renewable Energy Sources at the University Magdeburg where he completed his Ph.D. in 2007. From 2008 to 2021 he worked as a researcher in area of protection algorithms at Siemens Berlin. Since 2022 he is a Professor at the University of Applied Sciences Zittau/Görlitz on the Chair of Power System Protection and Network Operation.