Testing Transformer Differential Protection in Digital Substations

Use Cases and Results

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Objective

• **What** – Learning how to perform acceptance testing of SV Based transformer differential relay and understand the challenges and solutions

• **Why** – Because of standard protocols and digitization in substation

• **How** – Three test scenarios to compare analog based and SV based transformer differential
Introduction: Traditional Transformer Diff

- Internal Transducers
- Analogue Signal Processing (Filters, amplifiers etc.)
- Analog to Digital converter
- Digital signal processing (DSP), CPU etc.
Introduction: Sampled Values Transformer Diff

- **Merging Unit**
  - Internal Transducers
  - Analogue Signal Processing (Filters, amplifiers etc.)
  - Analog to Digital converter

- **Time Synchronization source**

- **Protection Relay**
  - Internal Transducers
  - Analogue Signal Processing (Filters, amplifiers etc.)
  - Analog to Digital converter
  - Digital signal processing (DSP), CPU etc.
- Dyn1
- Two-Winding Dual Slope % Restrained Differential
- Minimum Pickup = 5%
- High Set-point = 500%
- Slope-1 = 30%
- Slope-2 = 100%
• Low Staged Differential Trip for an in-zone fault
• High Staged Differential Trip for an in-zone fault
• \(2^{\text{nd}}\) Harmonic Restraint Element Operation for Inrush
Test Set up : Test Scenario 1

Protection Relay (Device under Test)

BIO

CT inputs

BIO – Binary Input Output channel

Test Set
Test Set up : Test Scenario 2

Protection Relay
(Device under Test)

BIO

NIC Port

Boundary Clock

Managed Network Switch

Transparent clock

Ordinary clock

Test Set

NIC Port

NIC – Network Interface Card
Test Set up: Test Scenario 3

Protection Relay (Device under Test)

CT Input  BIO  NIC Port

Boundary Clock

Transparent clock

Managed Network Switch

MU_9202

Ordinary clock

3

NIC – Network Interface Card

Test Set

3

BIO

NIC Port
## Results: Test Scenario 1

<table>
<thead>
<tr>
<th>Test</th>
<th>87T Trip Time (msec)</th>
<th>2\textsuperscript{nd} Harmonic detection (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Restrainted</td>
<td>Unrestrained</td>
</tr>
<tr>
<td>Test 1</td>
<td>25.7</td>
<td>20.1</td>
</tr>
<tr>
<td>Test 2</td>
<td>27.7</td>
<td>20.4</td>
</tr>
<tr>
<td>Test 3</td>
<td>28.1</td>
<td>20.7</td>
</tr>
<tr>
<td>Test 4</td>
<td>24.1</td>
<td>20.4</td>
</tr>
<tr>
<td>Test 5</td>
<td>28.8</td>
<td>19.1</td>
</tr>
<tr>
<td>Average</td>
<td>26.68</td>
<td>20.14</td>
</tr>
</tbody>
</table>
## Results: Test Scenario 2

<table>
<thead>
<tr>
<th>Test</th>
<th>Restrained (msec)</th>
<th>Unrestrained (msec)</th>
<th>2nd Harmonic detection (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test 1</td>
<td>29.5</td>
<td>19.6</td>
<td>5.1</td>
</tr>
<tr>
<td>Test 2</td>
<td>28.6</td>
<td>17.6</td>
<td>5.3</td>
</tr>
<tr>
<td>Test 3</td>
<td>28.0</td>
<td>19.8</td>
<td>4.9</td>
</tr>
<tr>
<td>Test 4</td>
<td>29.9</td>
<td>17.4</td>
<td>4.9</td>
</tr>
<tr>
<td>Test 5</td>
<td>30.1</td>
<td>18.2</td>
<td>4.0</td>
</tr>
<tr>
<td>Average</td>
<td>29.22</td>
<td>18.52</td>
<td>4.84</td>
</tr>
</tbody>
</table>
## Results: Test Scenario 3

<table>
<thead>
<tr>
<th></th>
<th>87T Trip Time (msec)</th>
<th>2nd Harmonic detection (msec)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Restrained</td>
<td>Unrestrained</td>
</tr>
<tr>
<td>Test1</td>
<td>27.1</td>
<td>20.9</td>
</tr>
<tr>
<td>Test 2</td>
<td>28.4</td>
<td>20.6</td>
</tr>
<tr>
<td>Test3</td>
<td>25.6</td>
<td>21.1</td>
</tr>
<tr>
<td>Test 4</td>
<td>27.8</td>
<td>20.9</td>
</tr>
<tr>
<td>Test5</td>
<td>28.5</td>
<td>21.1</td>
</tr>
<tr>
<td>Average</td>
<td>27.48</td>
<td>20.92</td>
</tr>
</tbody>
</table>
Results : Analysis

Restrained Trip times (msec)
COMTRADE : Test Scenario 2
Test Scenario 3: an additional GOOSE data attribute LD0.TR2HPDIF1.Op.general (unrestrained 87T trip) was used for timing tests and results are compared against TR2PTC GOOSE trip.
Performance of the network and redundancy are critical to the overall performance of protection and control systems that are process bus driven.

Per IEEE PES PSRC WG K15 – to clear a fault within 80-100msec; a communication signal must propagate within 5-10msec; these are met when conventional and non-conventional inputs are used.
Questions??