Testing IEC-61850 Sampled Values-Based Transformer Differential Protection Scheme

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Abstract— **Following the successful implementation of IEC 61850 at station level over the last decade and enough user-experience on the standard, the significance of process-oriented communication using process bus is on an exponential rise. One of the key components of a process bus is information exchange among the devices through Sampled Values. Sampled Values (SV) are used for transmitting digitized values of currents and voltages on ethernet frames. With increase in industry acceptance of SV compliant protective relays, there is a crucial need for testing these relays and systems to ensure they meet operational and commissioning standards.**

Functional testing of SV-based protective relays with the help of a test equipment that can publish SV streams can be seen as a first step. This paper will discuss in detail on how to test through fault conditions, pick-up, slope characteristics, and harmonic restraints on a transformer differential relay that utilizes process bus to subscribe to current samples. Additionally, this paper will also discuss the effect of network anomaly and the importance of time synchronization in a process bus-based transformer differential scheme.

Keywords— Transformer Differential Protection, Process Bus, Hybrid Protection, Centralized Protection, IEC 61850 9-2 Sampled Values, Nyquist Shannon theory

I. INTRODUCTION

Transformer Differential Protection (IEC: PTDF, ANSI: 87T) that operates on dual-slope characteristic is almost ubiquitous and its principles are well proven for various operating scenarios. While the low-stage (restrained) element of the 87T can provide security against CT mismatch and transformer tap changer errors and, in some cases, even CT saturation caused as an effect of through faults of large magnitude, the high-stage (unrestrained) element provides dependability for in-zone faults. Even order harmonic detection to inhibit blocking of low-stage has been quite popular method to detect magnetizing in-rush conditions. Out of all the even harmonics, 2nd harmonics are the most prevalent. Because of this fact, the paper will focus only on 2nd harmonic restraint.

In modern day digital substation environment with the implementation of IEC 61850 9-2 (Ed.2), several process bus driven architectures are proposed that provide significant reduction in copper wiring, facilitate ease of maintenance, thereby providing reduction in capital expenditure as well as operational benefits. In any process-bus architecture, a merging unit aggregates analogue and discrete signals and publishes digitized streams to various protection & control devices. This paper strives to provide findings on the performance of 87T protection element operation that utilizes sampled values (SV) and compares the performance with 87T element wired to conventional CTs. In addition, certain recommendations are put forth for consideration while designing fully process bus driven protection and control systems as well as hybrid systems that partially utilize process bus data while still relying on conventional as well as non-conventional instrument transformer connections.

Most internal functions of a microprocessor relays can be represented with a block diagram represented in Figure 1. Protection, communication, data logging and control functions are performed by Central Processing Unit (CPU), in some cases the communication processing may be performed by a different CPU.

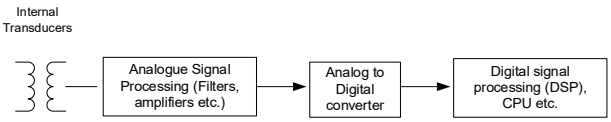

Figure 1 - Microprocessor relay functions

In process bus systems, the protection and other functions are performed remotely, and the functions can be represented as shown in Figure 2.

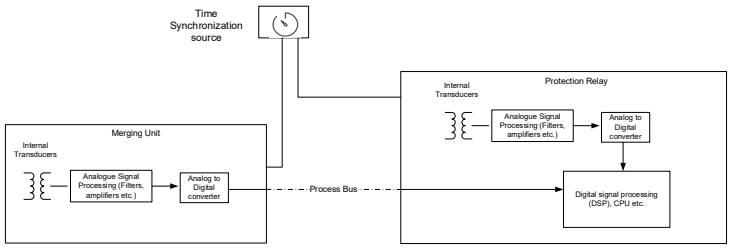

Figure 2 - Process Bus Systems

With digitization occurring at merging unit and subsequent re-sampling occurring at protection relay, high accuracy time source is required to accurately sample and utilize data for protection. Timing source have evolved from 1PPS to IEEE 1588v2 and several other means are available which utilize GPS/ Glonass constellation as time reference.

IEC 61850 9-2 LE implementation mandates 80 samples per cycle that translates to 4800 samples per second for 60 Hz

system, and 4000 samples per second for 50 Hz system. IEC 61850 9-2 LE requires PPS to be used as timing source protocol. However, with the acceptance of IEEE 1588v2 across the industry due to its benefits over 1PPS & IRIG-B such as its availability on managed ethernet switches, several process bus systems are utilizing it as a de-facto standard for time synchronization.

An IEEE-1588 enabled switch can be either a transparent clock (TC) or a boundary clock (BC). Using it as a transparent clock, the switch can monitor the ingress and egress PTP message and provide hardware timestamping, thereby publish the time delta in correction field. The ordinary clocks can utilize the correction field data and apply any offset to their respective internal clocks, hence achieving greater degree of accuracy with respect to the Grandmaster clock (GMC)/ Master clock.

Due to a high accuracy time synchronization source requirement for Sampled Value based protection applications, in this paper the protection relay itself used to synchronize the merging unit(s) and test set by means of IEEE1588 – Precision Time protocol (PTP) and no GPS enabled satellite clock were utilized. This setup provides a proof-of-concept that in the event a Grandmaster clock source is unavailable, the relay can serve as a backup Master clock.

The paper is divided into the following sections -

a) Test Scenarios and system Parameters – In this section, three scenarios based on the system design are discussed - i) analog signals on both windings of 87T, ii) SV streams from merging units on both windings of 87T and iii) hybrid of analog signals and merging unit (SV streams) on either winding of 87T. The behavior of protective relay performance is compared in each case. Protective relay settings considered as base reference are also provided.

b) Traditional Transformer Differential Vs SV Based Differential: Theory of Operation – In this section, theory of operation behind the considered transformer differential scheme is explained. Details of test set up used for each scenario is provided along with the calculations of test values used for each test type. Test results are provided for up to five tests under each test type and subsequently analyzed.

c) Test Analysis and Results – This section will cover the results for all the test scenarios and case types and a detailed analysis will be done

Recommendations and Conclusion – Based on the test results, a comparison is drawn between the performance of various scenarios and test types keeping results of traditional analog differential as a benchmark. Additionally, a GOOSE data attribute programmed for 87T trip was compared against the dedicated IED GOOSE trip signal for the scenario with hybrid signals to validate the performance and provide recommendations.

II. TEST SCENARIO AND SYSTEM PARAMETERS

Figure 3 shows the transformer under consideration for which the protection functions under test are highlighted. The CT Ratios are arbitrarily chosen, and the transformer construction is Delta-Wye grounded with phase shift of 30° with primary side leading.

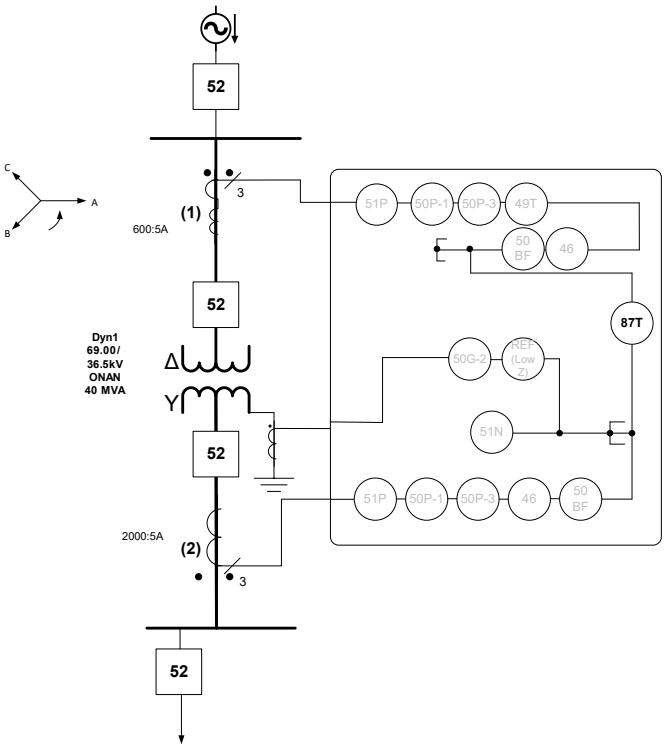

Figure 3 - Scenario 1 - Traditional Analog Differential Scheme

Using these system parameters two additional test cases are derived which utilize merging units to publish SV streams. Figure 4 shows MU_9201 and MU_9202 current merging units which publish SV Streams to the 87T and the Figure 5 shows only MU_9201 publishing SV stream & a bushing CT that are utilized for 87T Protection, which represents hybrid protection systems.

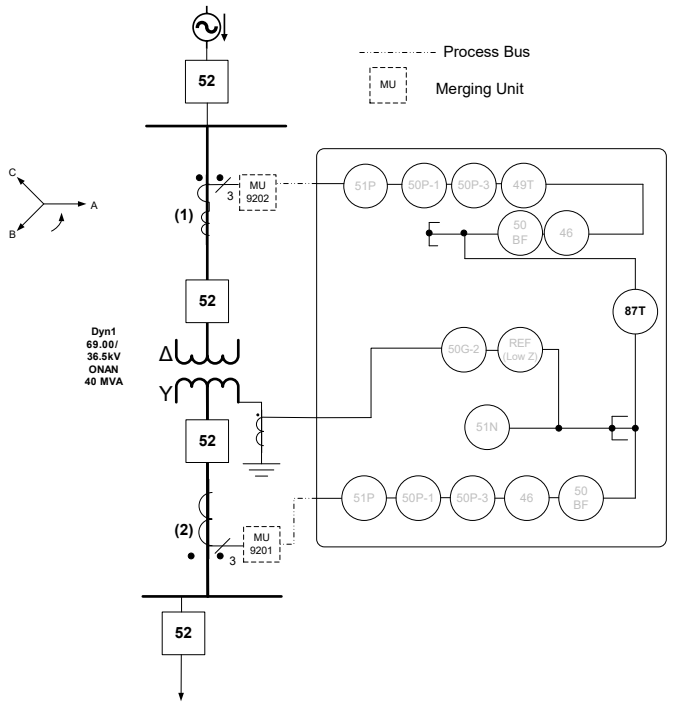

Figure 4 - Scenario 2: SV Based Differential Scheme

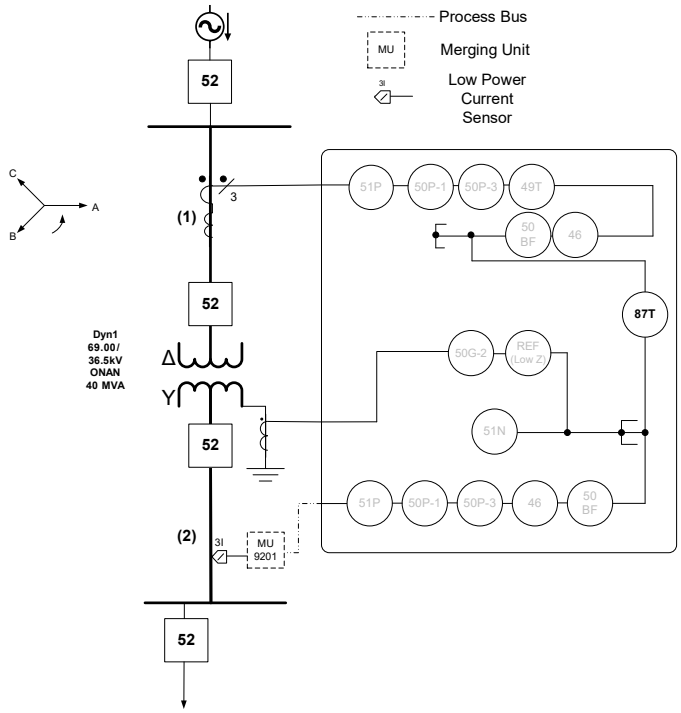

Figure 5 - Scenario 3: Hybrid Differential Scheme

Scenario: 3 presents challenges to the sampling and filtering mechanics in the relay and the test results are compared with Scenario:1.

A. *Multi-Rate Sampling*

To comprehend the execution of Scenario: 3, it is crucial to understand the concept of multi-rate sampling. A protection relay may receive current and voltage data from different secondary instruments – conventional instrument transformers (CIT), non-conventional instrument transformers (NCIT) as well as merging units which are connected to CIT and NCIT. Protection relays may need to accommodate all different types of sampling frequencies from different current and voltage sources. For instance, per IEC 60044-8, the rated value of NCIT's output data rate can be 1000Hz, 2400Hz or 4000Hz (for 50Hz systems). A merging unit per IEC 61850 9-2 publishes SV stream at 80 samples per power system cycle which translates to 5 Mbit/sec traffic on ethernet port of the subscriber. Protection relays receiving this data must be able to sample/ re-sample phasors by deriving fundamental frequency, harmonic content. A continuous digital low pass filter based on time domain continuous finite impulse response filter can be used. However, all techniques would still need to adhere to the Shannon-Nyquist theorem, which states that the sampling frequency should be at least twice the highest frequency contained in the signal, in mathematical terms:

$$fs \geq 2\,fc$$

fs – sampling frequency

fc – high frequency contained in the signal

NCIT are known to provide wide range of harmonic content and a merging unit connected to NCIT should also be able to adhere to Shannon-Nyquist theory if it were to be publish SV streams with greater resolution of harmonic content which can be utilized by protection relay for purpose of filtering power system transients.

B. *Settings*

Considering the CT ratio correction are 1.0 on both sides of the winding, the settings identified in Figure 6 are utilized for all test cases. The settings are programmed in terms of %Ir which indicates the percentage of rated current. To the plot between Id (diff. current) Vs. Ib (biasing current) is shown to the right-hand side of the figure. The operation of the 87T is verified against this to ensure erroneous operations are identified.

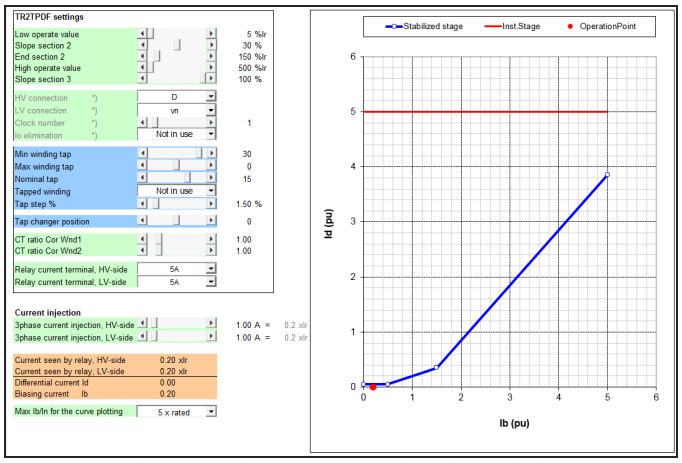

Figure 6 - Settings & 87T Operation Characteristics

III. TRADITIONAL TRANSFORMER DIFFERENTIAL VS SV BASED TRANSFORMER DIFFERENTIAL: THEORY OF OPERATION

A. Implementation of Traditional Transformer Differential

As discussed earlier, the transformer differential protection that has been considered in this paper uses a two staged percent differential scheme.

The biased low stage provides a fast clearance of faults while remaining stable with high currents passing through the protected zone increasing errors on current measuring. The second harmonic restraint ensures that the low stage does not operate due to the transformer inrush currents. The fifth harmonic restraint ensures that the low stage does not operate on apparent differential current caused by a harmless transformer over-excitation.

The instantaneous high stage provides a very fast clearance of severe faults with a high differential current regardless of their harmonics.

Both elements – low staged and high staged – operate phase-wise on a difference of incoming and outgoing currents. The differential current Id is a vector sum of winding-1 (Iw1) and winding-2 (Iw2) currents.

$$Id = |\overrightarrow{Iw1} + \overrightarrow{Iw2}|$$

The stabilizing current I_{bias} (Ib) of the protection relay in question uses the formula:

$$Ib = |\overrightarrow{Iw1} - \overrightarrow{Iw2}|/2$$

Figure 7 provides the parameters that were used in this example. The calculated currents and phase angles to be injected are shown below.

Low Stage Minimum Differential Pickup = 5% x Rated current, since the rated current is considered equal to the nominal current.

Low Stage Minimum Differential Pickup= 5% x 5A (Secondary) = 0.25 Amps

High Stage Unrestrained Differential Pick-up = 500% x 5 = 25 Amps (Secondary)

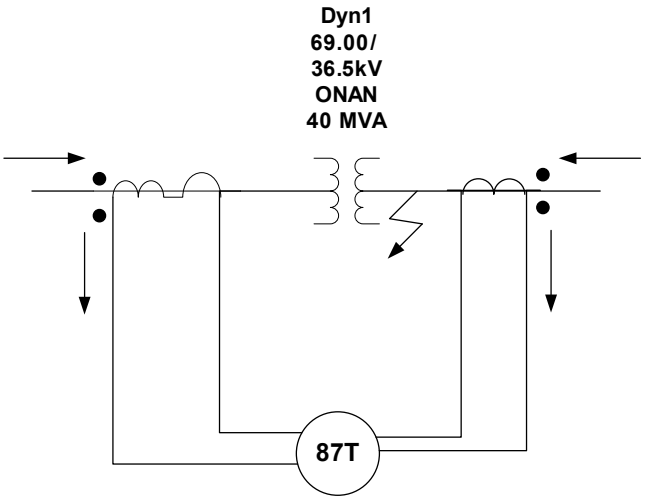

Figure 7 - Differential Scheme Under Test

Based on Figure 7, it is evident that there has to be 180-degree phase shift on winding-2 currents with respect to winding-1 to simulate an in-zone fault condition. In addition to that, the effect of phase shift due to the transformer connection has to be considered. A connection type of Dyn1 will introduce 30 degrees on winding-2. Test phase angles should add -30 degrees on winding-2.

Test Case-1: Low Staged Differential Trip for an In-Zone Fault

To obtain trip time, the test was run with pre-fault and fault states. During the pre-fault, the system under normal load conditions was simulated for 3 seconds. A low staged differential condition was simulated in the fault state. Currents I1, I2, and I3 were injected into winding-1 whereas I4, I5, and I6 into winding-2 respectively.

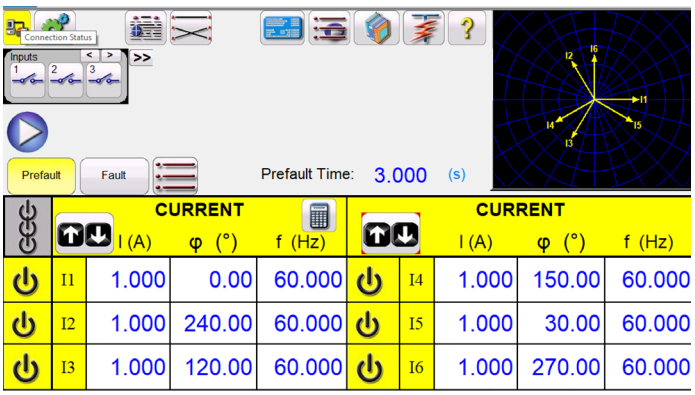

Figure 8 - Pre-Fault State

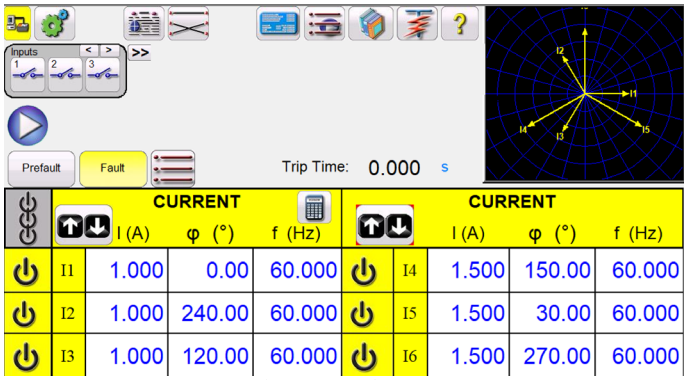

Figure 9 - Fault State

Test Case-2: High Staged Differential Trip for an In-Zone Fault

Similar to Case-1, both pre-fault and fault states were simulated to reflect an actual power system phenomenon. A high staged differential condition was simulated in the fault state.

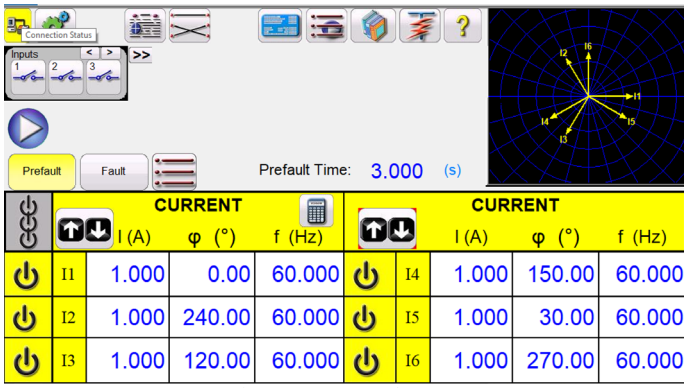

Figure 10 - Pre-Fault State

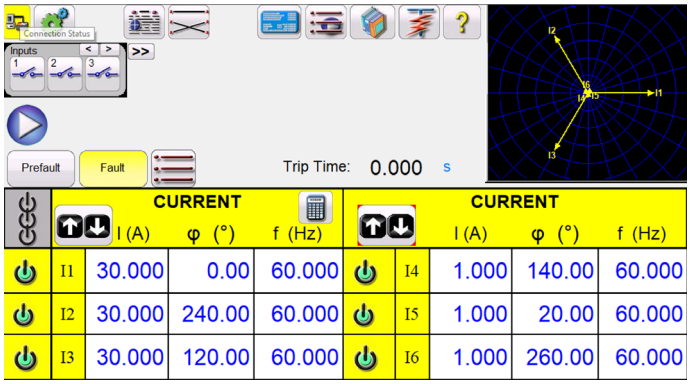

Figure 11 - Fault State

Test Case-3: 2nd Harmonic Restraint Element Operation for Magnetization Inrush Condition

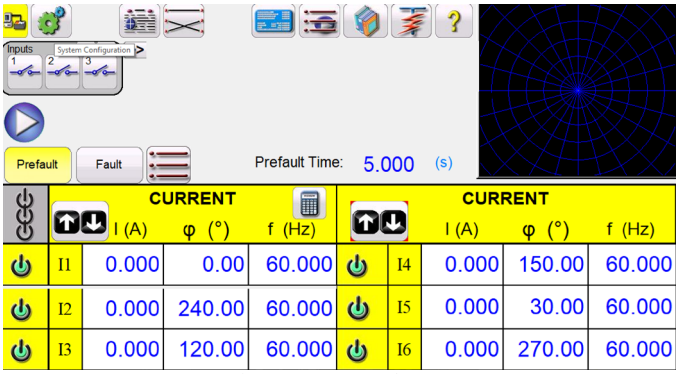

Figure 12 - Pre-Fault State

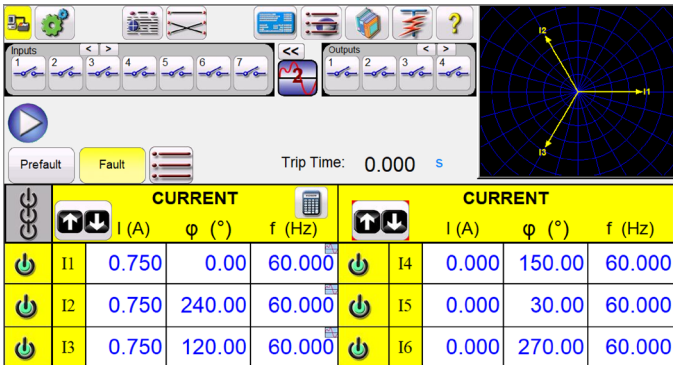

Figure 13 - Fault State

Test System Set-up

Timing tests for 87T operations were recorded using analogue (hard-wired) I/O, timing tests for 2nd harmonic restrain pickup were recorded internally in the protection relay. Binary input was programmed to start oscillography recorder when 2nd harmonic currents were injected. The time delta was calculated when 2nd Harmonic block picked up. Considering that the harmonic restrains are internally utilized within the 87T element, utilizing a binary input wired to test set to calculate time delta would add additional delays. Hence a simplified test methodology was utilized. A high-speed output was mapped to 87T trip in the protection relay.

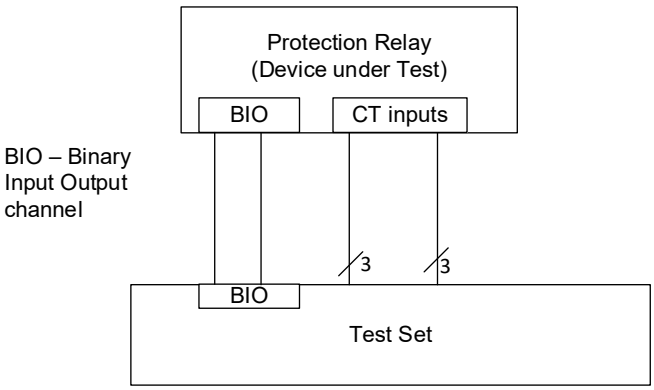

Figure 14 - Test Setup - Scenario 1

B. *Implementation of SV-Based Transformer Differential (Scenario:2)*

Similar to traditional scheme with purely analog inputs, this test scenario employed Sampled Value streams (SV) and GOOSE messages to measure the performance of the relay. For time synchronization purposes, IEEE 1588 protocol was selected. The relay served as the boundary clock (without GPS tracking), and the test equipment synchronized to the relay. Being IEEE 1588-synchronized to the relay, the test set simulated two Merging Units by publishing two SV streams. The first stream simulated the three currents from the primary winding, and the second stream simulated the three currents from the secondary winding. With the help of a Managed Network Switch, all the SV frames and GOOSE traffics were exchanged between the test set and the relay. The relay subscribed to two SV streams and was programmed to publish the GOOSE carrying trip command to the test set.

Once the network setting up was done, testing became as seamless as it was with analog injection. Two Sampled Values streams carrying prefault currents for 5 seconds were injected into the network. The test set then changed quantities to a fault condition and started the timer. The relay tripped and sent out a trip GOOSE. Monitoring the trip GOOSE from the relay, the test set stopped the timer and reversed the fault quantities to normalized quantities. Test times are recorded below:

Test System Set-up

Testing for this case involved using a test set that was synchronized to the protection relay using IEEE 1588 PTP and published SV Streams. IEC 61850 GOOSE message was used as a trip signal from the relay to the test equipment to perform harmonic restraint and 87T timing tests. A general Trip LD0.TR2PTRC1.Op.general (General Protection Trip) was mapped to publish Trip when 87T tripped.

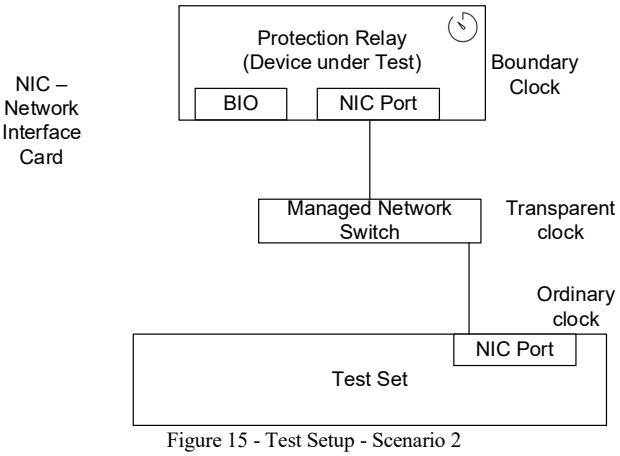

Figure 15 - Test Setup - Scenario 2

C. *Implementation of Hybrid Transformer Differential (Scenario:3)*

This test scenario employed the hybrid signals. To achieve this objective, the test set mainly injected 6 analog currents. Three of the six analog currents were connected straight into the relay as if they were from the primary winding of the transformer. The other three analog currents were connected into the Merging Unit (MU). Synchronized to the relay via IEEE 1588, the MU translated the three analog currents into one SV stream and published it to the relay. Effectively, the relay took three analog currents and three SV-based currents as input for transformer differential protection. The test set is subscribed to the trip GOOSE being sent out when the simulated fault condition occurred.

Considering the hybrid nature of this setup, an analogue method – like what was utilized in Scenario- 1 it was decided to hard-wire contacts to measure the 87T trip time. One set of test currents were injected into protection relay and another set was injected into the merging unit. A high-speed output on relay was programmed to trip on 87T operate and was wired to the binary input of the test set.

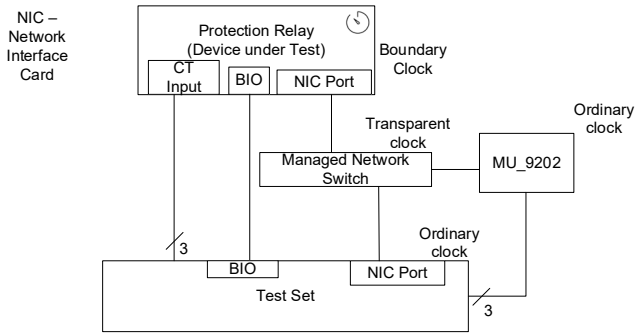

Figure 16 - Test Setup - Scenario 3

IV. Test Results and Analysis

Timing tests were performed for each test case, these tests include five iterations for restrained operations and five iterations for unrestrained operation. Five additional timing tests were run to determine the 2nd harmonic pickup timing. A managed network switch with hardware PTP implementation was set to be a transparent clock and the protection relay was set to be a boundary clock to synchronize the other merging unit(s) and Test set. Traffic prioritization and network segregation were not performed.

Test currents were injected at random phase angle in all the iterations. For the restrained case the differential current of 2 time the set value was injected and for unrestrained cases a differential current of 5.8 times of the rated current was inject.

Table 1 - Results Test Scenario 1

		87T Trip Time (msec)		2nd Harmonic detection (msec)
		Restrained	Unrestrained	
Scenario- 1	Test 1	25.7	20.1	4.167
	Test 2	27.7	20.4	6.25
	Test 3	28.1	20.7	6.25
	Test 4	24.1	20.4	6.25
	Test 5	28.8	19.1	4.167
	Average	26.68	20.14	5.41

Table 2 - Results Test Scenario 2

		87T Trip Time (msec)		2nd Harmonic detection (msec)
		Restrained	Unrestrained	
Scenario - 2	Test 1	29.5	19.6	5.1
	Test 2	28.6	17.6	5.3
	Test 3	28.0	19.8	4.9
	Test 4	29.9	17.4	4.9
	Test 5	30.1	18.2	4.0
	Average	29.22	18.52	4.84

It is observed that when compared to scenario 1, the deviation of the average for restrained pickup is within 2.5 ms and well within the published maximum operation times of the protection relay. This minor deviation can be attributed a few factors – no prioritization and segmentation between GOOSE and SV traffic and the fault was injected at an arbitrary phase angle.

Table 3 - Results Test Scenario 3

		87T Trip Time (msec)		2nd Harmonic detection (msec)
		Restrained	Unrestrained	
Scenario 3	Test1	27.1	20.9	8.3
	Test 2	28.4	20.6	8.5
	Test3	25.6	21.1	7.4
	Test 4	27.8	20.9	8.6
	Test5	28.5	21.1	7.9
	Average	27.48	20.92	8.14

The deviation in average for restrained pickup between scenario 3 and scenario 1 is marginally better in scenario 3. It was observed that the waveform from merging unit was re-sampled and aligned in the protection relay to provide dependable protection. The average of the harmonic restrain pickup was observed to be 2.72 msec faster than Scenario- 3, this is attributed to the additional security built into the protection relay algorithm to accurately detect magnetizing inrush by taking he ratio of the 2nd harmonic differential current with the fundamental differential current. Considering that deviation in average trip times are within 1.5 msec, it is noted that harmonic restrain doesn't compromise the dependability of the protection as the protection is still operating within published margins.

A line graph is plotted for restrained trip times for visual comparison in Graph 1, it is noted that for biggest deviation is observed for iteration 4 of case 2 and the Comtrade capture for this case shows that unrestrained element operated in 21.35 msec. The additional time observed is the processing time for GOOSE publishing, network propagation delay and GOOSE subscription time.

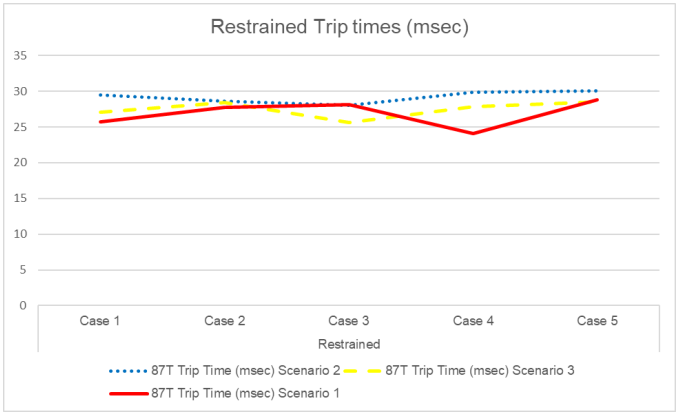

Figure 17 - Restrained Trip Times (msec)

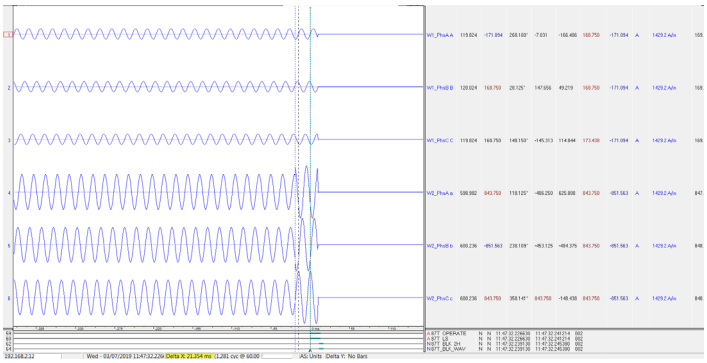

Figure 18 - Comtrade Case 2 - Iteration 4

V. Recommendations

Performance of the network and redundancy are critical to the overall performance of protection and control systems that are process bus driven. Traffic prioritization and management on network switches becomes critical for guaranteed service to protection traffic. [4] is a technical report which documents the guidelines for communication network and systems engineering. Methods for testing loss of packet(s) and their impact on protection and control systems need further refinement. IEC 61850 station bus engineering also requires due engineering diligence. While performing testing on case 3, an additional GOOSE data attribute LD0.TR2HPDIF1.Op.general (unrestrained 87T trip) was used for timing tests and results are compared against TR2PTC GOOSE trip.

Table 4 - TR2PTRC vs TR2HPIF Timing

	TR2PTC GOOSE timing (msec)	TR2HPDIF - GOOSE timing (msec)
Iteration 1	20.0	18.3
Iteration 2	19.7	18.3
Iteration 3	20.4	18.3
Iteration 4	20.0	19.8
Iteration 5	19.9	19.1

TR2HPDIF operating times are marginally better, since the TR2HPDIF had a higher execution priority in the relay.

VI. Conclusions

Fundamental concepts of using SV for protection of fully digital transformer differential protection as well as semi-digital (hybrid) protection are proven by test cases and corroborated with results and COMTRADE analysis. It is observed that the relay protection can propagate communication signals (GOOSE) within 5msec and consequences of loss of Grandmaster clock synchronization can be mitigated by using a relay as a back-up master clock. The average operation time of the protection (87T) was found to be well within the relay manufacturer published data regardless of whether the input was derived from conventional CT's or merging unit as analyzed by comparing results from Scenario: 1 with Scenario: 2 and Scenario: 3 individually.

VII. References

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