CVT Transients - Causes, Effects and Solutions

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***Abstract*—The conceptual design of capacitor voltage transformer(CVT) was proposed as an alternative to standard electromagnetic voltage transformer in 1936 and analysis were made to understand the performance of CVT in 1949. Ever-since the introduction, many field issues were reported which led to the birth of working group on transient characteristics of capacitance potential devices. Distance relay mal-operation due to potential device transients was first suspected in this AIEE committee report in 1951.**

Even though transient phenomenon in coupling-capacitor voltage transformer (CCVT) was persisting before, it was not brought to notice due to the slow response time of electromechanical relays. The introduction of solid state, digital and numerical relays offered half to one full cycle range high speed tripping which really exposed the CVT transients to the protection world. Efforts were then made to understand the transient performance of CCVT.

In this paper, we discuss the ferro-resonance problem and practically available solutions for ferro- resonance problem i.e. ferro resonance suppression circuits (FSC). We then discuss the transient performance of each FSC and their impact on distance zone 1 reach. This paper also provides information about practical solutions available and recommendations for each kind of FSC.

I. Introduction

Protective relay acts as a backbone to power system. A century old protection has recently stepped into fourth generation technology, a massive development from electromechanical to static, static to digital and from digital, numerical to wide area protection. The very first relays which were introduced were of the electromechanical type having tripping time in the order of few hundreds of milliseconds. Even though these relays have high operating time when compared with modern digital and numerical relays, they were able to meet the system needs in those periods. In order to meet the rapid growth demand and to ensure reliability, the power system was made to operate in an interconnected fashion, which led to other issues like stability, system availability during disturbances. This demanded high speed fault clearing times inorder to ensure stability and minimze damages to electrical equipment which were feeding the fault.

Protective relays play a vital role in fault clearing process. The fundamental task of protective relay is to extract the desired information from the first post fault cycle and utilize it to detect and classify different fault types occurring in power system and to send control signal i.e., trip signal to the circuit breaker to isolate the faulted phase/network. In addition to circuit breaker operating time, fault detection and classification contribute a significant portion to the total fault clearing time. This involves signal processing delays to process the voltage and current information obtained via instrument transformers and other adaptive delays introduced, if any, to ensure secured relay operation.

The major task of this signal processing unit is to extract the desired information in the presence of noise so that the extracted information can be later processed by algorithms to achieve the desired control action. Power system faults are typically accompanied by transients and this poses a challenge to the signal processing unit to extract the desired information without sacrifying accuracy and speed.

The instrument transformers plays a crucial role in the entire chain i.e., to mirror the primary voltage and current information without adding any noise to protective relays. However, noise introduced by instrument transformers e.g. current transformer (CT) saturation, capacitor voltage transformer transients (Fig. 1) poses challenge to high speed protective relays, which is the focus of this paper.

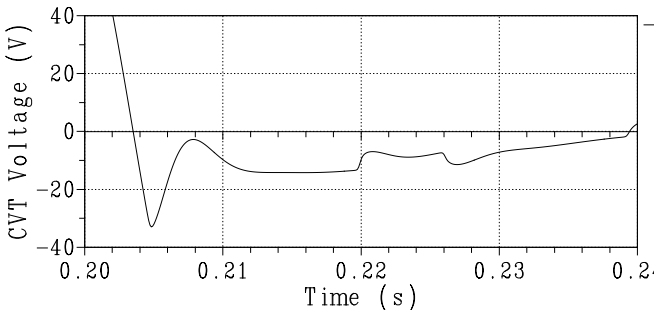

Fig. 1. CVT response in the presenece of primary arc

II. Capacitor Voltage Transformer

The term ”capacitor voltage transformer” (CVT) was first introduced in 1936 as an alternative to electromagnetic voltage transformer primarly for synchronisation and relaying application [1]. As the use of CVT instead of electromagnetic voltage transformer can result in considerable savings, particularly for high-voltage systems, efforts were made to analyze the performance of CVT and to improve the design to meet the ratio and phase angle errrors under vayring operating conditions [2]. Fig. 2 shows the detailed model of CVT, which consits of capacitor voltage divider, compensating reactor to overcome the voltage drop and to improve the performance of capacitor voltage divider by tuning the reactor at the supply frequency i.e. reactor must be in resonance with the sum of the two capacitances so that primary voltage and the current are in phase as shown in Fig. 3. As the resistance in the voltage divider can result in significant impact on accuracy, intermediate transfomer is introduced to improve the performance.

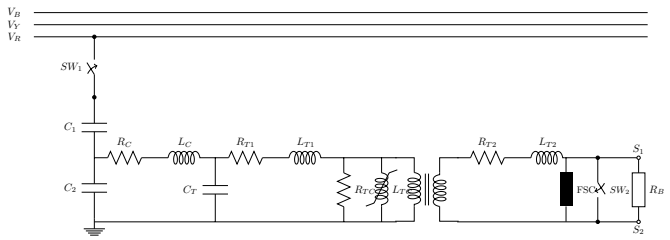

Fig. 2. Detailed model of CVT

where,

C_1,C_2	capacitor voltage divider
R_C,L_C	tuning reactor resistance and inductance
C_T	stray capacitance of step down transformer
RT_1,RT_2	primary and secondary winding resistance of intermediate transformer
LT_1,LT_2	primary and secondary winding leakage inductance of intermediate transformer
R_{TC}	resistance representing core loss of intermediate transformer
L_{TC}	magnetising inductance
R_B	Relay burden
SW_1,SW_2	Switches
FSC	Ferro resonance suppression circuit

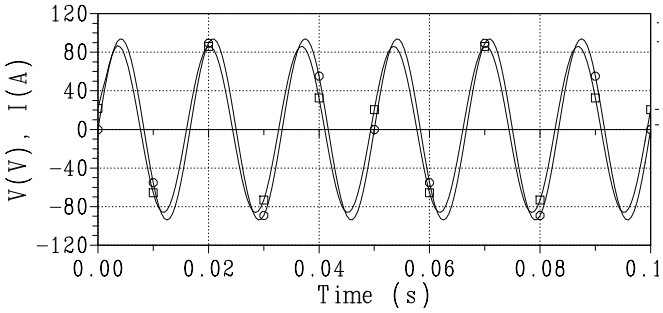

Fig. 3. Primary voltage (square) and current (circle, scaled) in the presence of compensating reactor

A. Understanding Ferro-resonance

The term ferro-resonance dates back to 1920 [3] which refers to a oscillation between capacitor and non-linear inductor. This phenomenon is a major concern to power system operators as it can result in large currents, which may overheat the windings and/or sustained or temporary overvoltages which may result in insulation breakdown leading to equipment failure. Depending upon the mode of oscillation, ferro-resonance oscillation can be classified as follows [4], [5],

- *Fundamental:* The oscillation(distorted waveforms) frequency is same as the system frequency
- *Sub Harmonic:* The period is integer multiples of source period
- *Quasi Periodic:* Unlike the above modes, where the signal is periodic, in quasi mode, it is not periodic with discontinous spectrum
- *Chaotic:* Oscillation is not periodic with continous spectrum

Different power system configuration can lead to ferro-resonance and it is not limited to CVT alone, for e.g. use of electromagnetic voltage transformer in isolated or resonant grounded networks or the interaction of voltage transformer with grading capacitors can lead to ferro-resonance i.e. any network/equipment which has the interaction between capacitor, voltage or current source and non-linear inductor can lead to ferro-resonance oscillation. In the case of CVT, all these exists, i.e.,

- Capacitor - capacitor voltage divider
- Non-linear inductor - saturation of the magnetic core of the intermediate transformer
- Driving source

1) Ferro-Resonance Test: Ferro-resonance test (FT) is conducted on CVT to ensure CVT design prevents sustained oscillations [6]. In order to understand the significance of ferro-resonant oscillation and supression circuit, FT is simulated using CVT model as shown in Fig. 2, without any FSC. This is done by closing the switch SW_1 permanently i.e. driving source and switch SW_2 is closed at 0.2s and opened after 100ms which is the minimum short-circuiting time as per standard [6], which mimics the operation of secondary protection device e.g. fuse. This drives the core into saturation leading to the interaction of non-linear inductor with capacitor resulting in ferro-resonance condition as shown in Fig. 4.

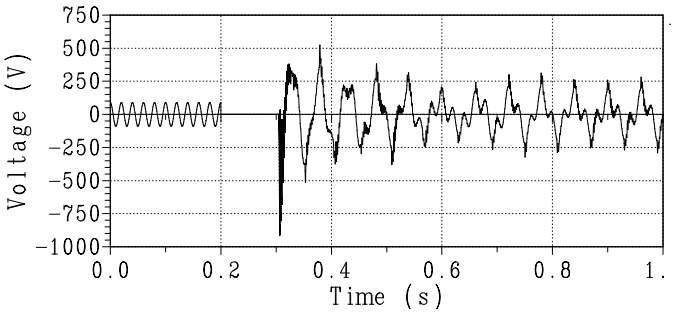

Fig. 4. CVT secondary voltage - without FSC

The sustained overvoltage condition can result in insulation breakdown leading to equipment failure. In addition to this, it may result in relay mal-operation.

Unlike linear resonance, where the response is predictable, ferro-resonance is not easily predictable as several stable operating points may exists for a particular excitation and a range of circuit parameters. Thus it is difficult to precisely predict and prevent ferro-resonant condition and the only option is to suppress the oscillation using ferro-resonance suppression circuit (FSC) which we will discuss in the later sections.

III. CVT Transients - Causes

Distance relay mal-operation due to CVT transients is first suspected when electromechanical relays were replaced by high speed relays. In 1948, the Carrier-current committee

referred CVT transient problem to the Joint Subcommittee on Instrument Transformers, which later appointed the working group, Transient Characteristics of Capacitance Potential Devices, which first met on October 27, 1948. In response to the questionnaire circulated to utilities [7], it was found that there were three noticeable problems due to CVT,

- improper tripping when a fault was in non-tripping direction
- delayed tripping when a fault was in the tripping direction
- improper tripping owing to protective-gap spark-over during disconnect-switch operation with no fault on the system.

Tests were conducted on CVT and analysis of the experimental test results indicates that power factor of the burden has more impact on the transients and high speed relay mal-operation. Analysis were also done on both phase and ground relay operations. Finally, the working group suggested either to use potential transformer, if it is economical or to improve the power factor of secondary burden to CVT by some additional means. This led to the root cause analysis of CVT transients, which identified the following factors contributing to CVT transients [8],

- Point on the primary, transmission line voltage wave where the fault occurs,
- Magnitude of tap and stack capacitance,
- Turns ratio of the intermediate voltage magnetic transformer,
- Type of ferro resonant suppression system (active/passive),
- Composition and connection of burden,
- Amount of resistance inherent in the potential device circuit,
- Exciting current magnitude of the intermediate voltage transformer,
- Magnitude and power factor of the potential device burden.

The following sub-sections provides brief overview of the above factors,

A. Point on wave

For a compensating reactor tuned at system frequency and for resistive or unity power factor burden, the primary current and voltage will be in-phase. However, the voltage across the capacitor or inductor will be 90 degrees out of phase with respect to current i.e., when the primary current goes zero the voltage across the capacitor will be maximum. Thus, the energy stored in capacitor ($\frac{1}{2}\mathrm{CV}^2$) will be maximum when the primary current/voltage goes to zero as shown in Fig. 5.

On the other hand, the energy stored in inductor ($\frac{1}{2}\mathrm{Li}^2$) will be maximum when the primary current goes maximum as shown in Fig. 6. Thus at any point of wave where the fault occurs we have some stored energy, which will appear as transients. The time constant of this transients can be analytically estimated using the connected burden information and this is estimated to be 31ms for the capacitance (fault at zero crossing) and 0.227ms for the inductance (fault at crest).

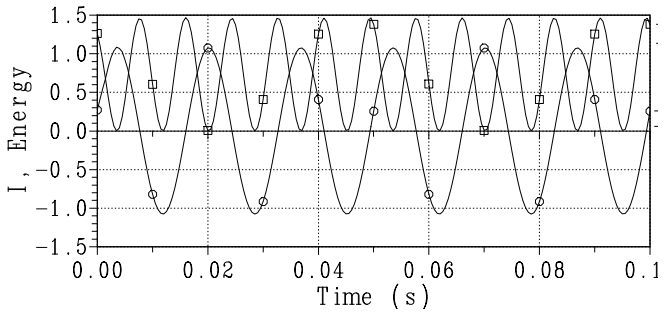

Fig. 5. Energy (square, scaled) stored in capacitor

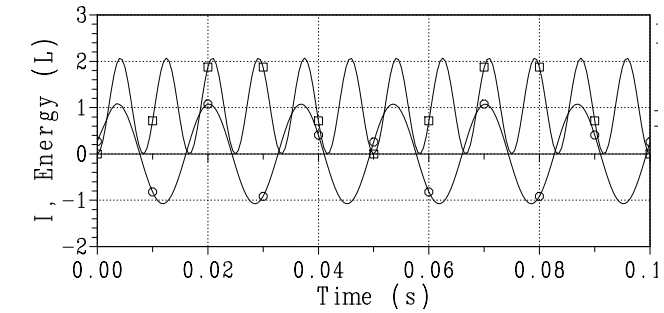

Fig. 6. Energy (square, scaled) stored in inductor

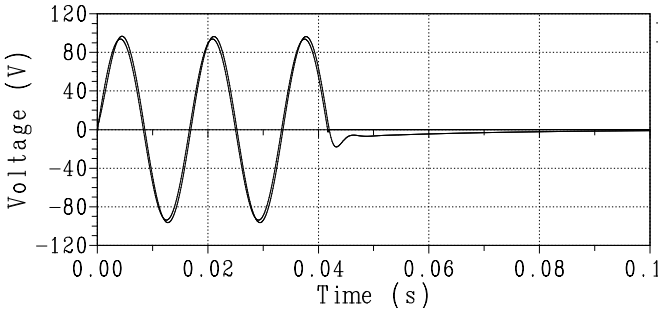

Fig. 7. Transients due to energy stored in capacitor for fault at zero crossing

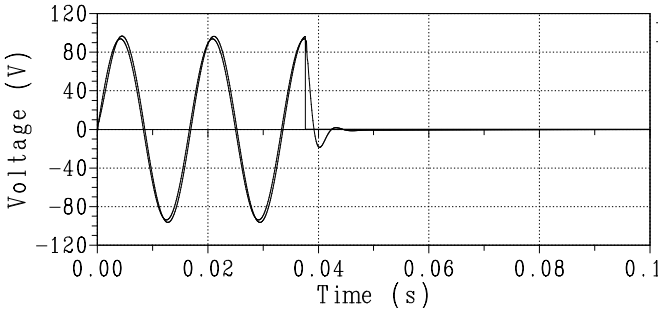

Fig. 8. Transients due to energy stored in inductor for fault at peak

Fig. 7 and Fig. 8 shows the transients in CVT secondary due to stored energy in capacitor and inductor respectively, where it can be observed that the analytically estimated values closely matches with the simulated values.

B. Magnitude of tap and stack capacitance

Let's assume we have a fixed burden connected to CVT secondary and the stack capactiance is increased. When the capacitance is increased, the capacitance reactance will decrease i.e. for fixed burden current the voltage drop across capacitor will reduce resulting in transient with decreased magnitude as shown in Fig. 9. However, as a tradeoff the duration of transient increases (τ=RC)

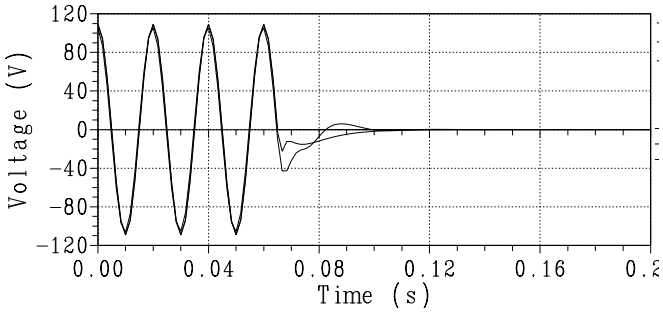

Fig. 9. CVT secondary voltage when the tap and stack capacitance is increased

C. Turns Ratio of Intermediate Transformer

We have observed that the capacitor induced transients has longer time constant. One way to reduce the energy, is to reduce the voltage across capacitor (IX_C), which can be achieved by reducing the primary current. This can be achieved when the turns ratio of intermediate transformer is increased.

D. Ferro-resonance Suppression Circuit

As discussed earlier, CVT's are prone to Ferro-resonance oscillation and suppression circuits are introduced to suppress these oscillation to avoid equipment failure. The simple and obvious option is to introduce the resistor to damp the oscillation. However, the insertion of resistor causes a continous loading effect during normal condition causing increased energy storage thereby resulting in more trasients for faults at zero crossing.

1) Active - Ferro resonance test [6]: Fig. 10 shows the digital model of active FSC which is connected to the secondary side of intermediate transformer (Fig. 2)

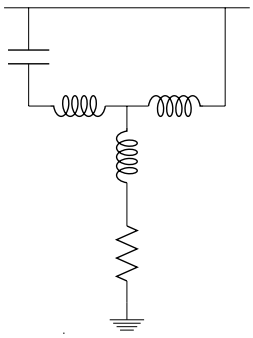

Fig. 10. FSC - Active Type

The filter is tuned in such a fashion that it has high impedance at fundamental frequency to avoid loading effect during normal operating condition and during offnominal frequencies i.e. during ferro resonance condition, the effective impedance approaches the resistive burden to damp ferro-resonance osciallation. Fig. 11 shows the performance of active FSC for ferroresonance test. It can be observed that the error after damping is less than 10% and it takes 129 ms (approx) which is less than 0.5s as per standard.

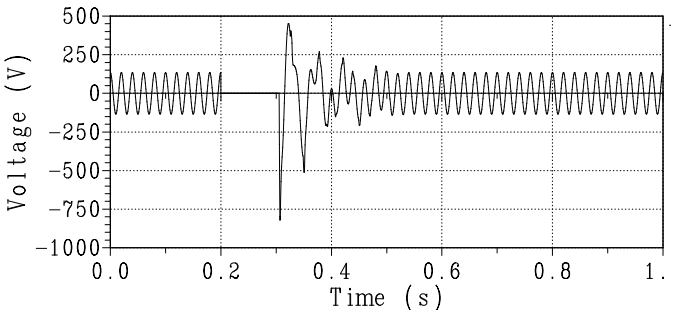

Fig. 11. CVT secondary voltage - with Active FSC (25% resistive burden)

2) Active - Transient Response Test [6]: As ferro-resonance test is conducted to ensure the damping of ferro-resonance oscillation, transient response test is conducted to ensure delivery of the desired actual primary information to the protective relay after a specified time interval. Different test cases like

1) bolted phase to ground fault at peak and zero crossing of primary voltage waveform
2) 25% and 100% of burden range I (1 VA, 2.5 VA 5 VA)
3) 25% and 100% of burden range II (10 VA, 25 VA, 50 VA, 100 VA)

are considered. Fig. 12 shows the transient response for the above mentioned cases.

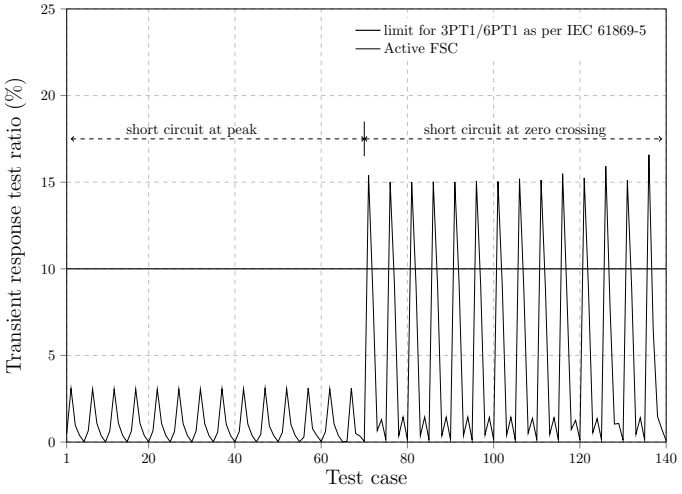

Fig. 12. Transient response test ratio - ActiveFSC

Transient response test ratio (TSTR) is calculated using

equation (1),

$$TSTR = \frac{|V_s(t)|}{\sqrt{2}V_p} \quad (1)$$

where

$V_s(t)$	secondary voltage at a specified time T_s after application of short circuit
$\sqrt{2}V_p$	secondary voltage peak before short circuit
T_s	10ms, 20ms, 40ms, 60ms, 90ms

This is required to ensure that the transients shall decay within the specified time T_s, to a specified value of the peak voltage before the application of short circuit.

3) Passive - Ferro resonance test [6]: Fig. 15 shows the digital model of passive FSC which is connected to the secondary side of intermediate transformer (Fig. 2). Energy storage elements responsible for CVT transients in active FSC are replaced by saturable inductor in series with a resistance in passive FSC so that more resistive burden is connected to CVT during ferro-resonance and during normal operating condition it provides high impedance to reduce loading effect.

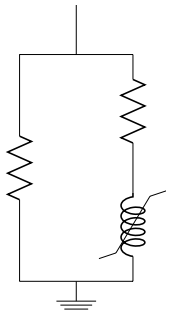

Fig. 13. FSC - PassiveType

The CVT with passive type FSC is designed to provide unity gain at fundamental frequency and to attenuate the unwanted information as shown in Fig. 14. This can be obtained using the detailed transfer function (Appendix A).

$$G(s) = \frac{N_3 s^3 + N_2 s^2}{D_5 s^5 + D_4 s^4 + D_3 s^3 + D_2 s^2 + D_1 s + D_0} \quad (2)$$

where $N_3, N_2, D_5, D_4, D_3, D_2, D_1$ are the coefficients expressed by CVT parameters

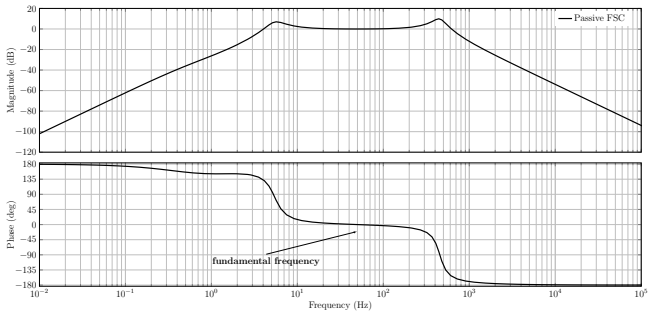

Fig. 14. Magnitude and phase response of CVT with passive FSC

Fig. 15 shows the performance of CVT with passive FSC connected to the secondary of intermediate transformer, where the 10% error condition is met in 9 ms after the short circuit is removed. Table I shows the compartive performance of both active and passive FSC for ferro-resonance test, where it can be observed that passive FSC is fast in damping the ferro resonance oscillations.

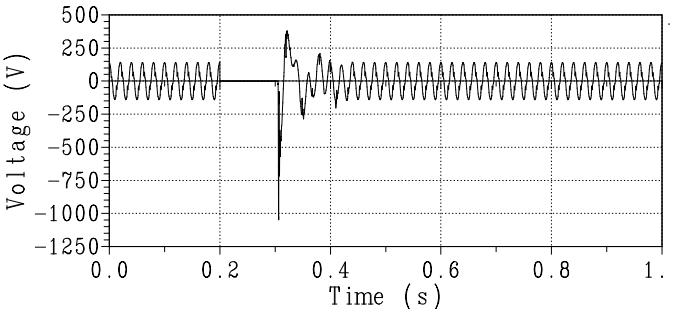

Fig. 15. CVT secondary voltage - with Passive FSC (25% resistive burden)

TABLE I
FERRO-RESONANCE TEST

FSC type	Recovery Time (ms)
Active	129
Passive	9

4) Passive - Transient resonance test [6]: The cases which were discussed in active section were considered with passive FSC. Fig. 16 shows the transient response test results of CVT with passive FSC where it can be observed that the irrespective of the test scenarios, the fault information delivered by CVT with passive FSC to protective relay is better than CVT with active FSC (Fig. 12)

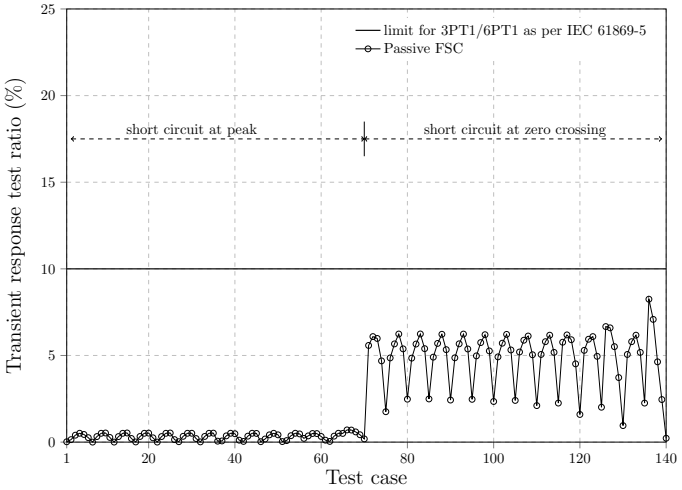

Fig. 16. Transient response test ratio - PassiveFSC

E. Stray Capacitance of Intermediate transformer

The other factor to consider is the stray capacitance of intermediate transformer primary winding. Fig. 17 shows the impact of varying stray capacitance on CVT magnitude response. It can be observed that there is a impact in magnitude

response when the stray capacitance is varied, however the impact is felt ouside the protective relaying filtering band.

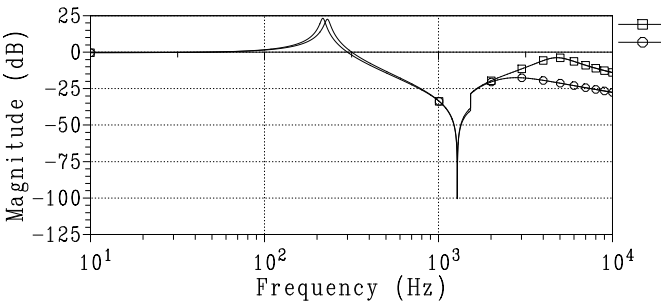

Fig. 17. Impact of primary winding stray capacitance on CVT magnitude response

IV. CVT Transients - Effects

Although the CVT is well designed to minize the impact of transients, the use of FSC introduces transients which impacts the performance of protective relays as the fault information is corrupted especially in the first post fault cycle. This results in overreaching issues casuing relay maloperation as shown in Fig. 18, where the estimated impedance causes zone 1 overreach for a zone 2 fault and moves away from the fault location (F) due to the elongation in primary arc.

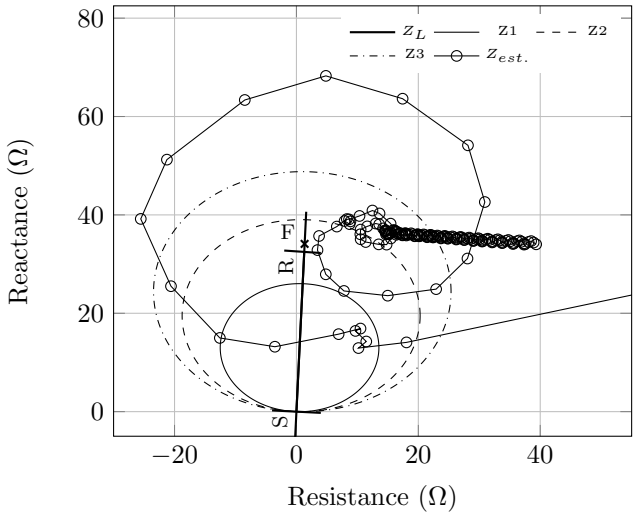

Fig. 18. Impedance plot for a single phase to ground fault

The problem of zone 1 overreach due to CVT transients is not new and is well document and discussed in literature [9], [10], [11], [12], [13] . Fig. 19 to 21 shows the safe zone 1 reach for a fault at 100% of line length for different fault types with both active and passive CVT. It can be observed that the problem of overreaching is more severe when active CVT's are used to provide the fault information. Looking into Fig. 19 to 21, it is not practical to set the zone 1 reach to a very low value to avoid relay mal-operation during high SIR condition. Next section discusses the practically available solutions to overcome the zone 1 overreaching issue.

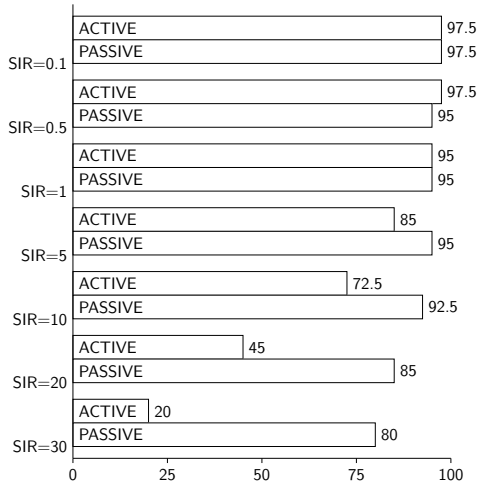

Fig. 19. Maximum Zone 1 reach for single phase to ground fault

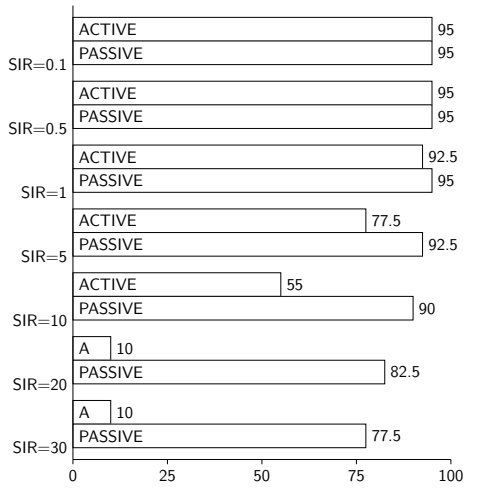

Fig. 20. Maximum Zone 1 reach for phase to phase to ground fault

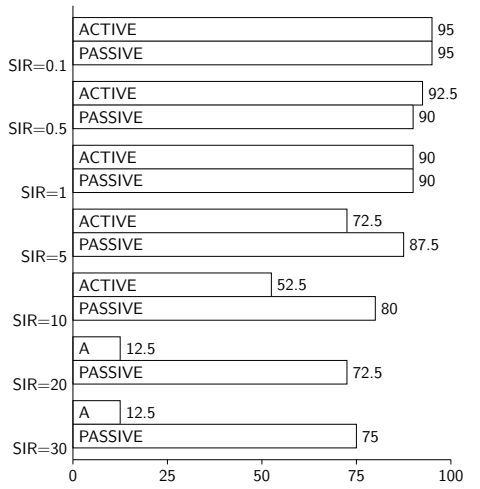

Fig. 21. Maximum Zone 1 reach for 3 phase fault

V. CVT Transients - Solutions

A. Reach Reduction

One obvious solution is to reduce the reach to avoid relay maloperation due to zone 1 overreach. This involves understanding the CVT response for different scenarios to arrive at a safe zone 1 reach. e.g. from Fig. 19 to Fig. 21 it can be observed that the safe zone 1 reach can be set to cover only 10% of protected line length i.e., instantaneous operation can be achieved for only 20% of the protected line and remaining 80% involves tripping time delay.

B. Fixed Time Delay

Another option is to provide a fixed time delay for zone 1 operation. However, there are two issues in this approach,

- Estimation of this time delay needs simulation studies involving multiple worst case scenarios to ensure that the time delay is more than the CVT transient duration
- Even in the absence of CVT trasients, tripping is delayed which may impact system stability

C. Adaptive Time Delay

One way to improve the tripping speed is to make the time delay adaptive, so that instantaneous zone 1 operation can be achieved for system scenarios which does not have significant impact on CVT transients. This is achieved by,

1) Extracted CVT Transients Information: Adaptive time delay can be achieved by indirectly monitoring the CVT transient information by filtering the signal e.g. digital mimic filter[14], double differentiator[15]. Fig.22 shows the response of digital mimic and double differentiator for voltage signal obtained from active type CVT model. Output samples are

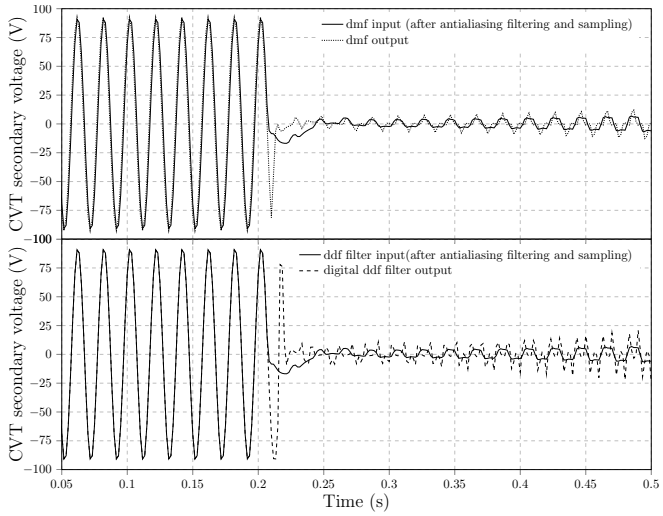

Fig. 22. Extracted CVT transient information using digital mimic and double differentiator

delay adjusted to show the filter performance and it can be observed that the output samples are not matching the input after CVT transients die out. This is due to the fact that, even though an indirect filter provides attenuation in the low frequency region it amplifies the signals above fundamental frequency.

To overcome this, other filters like feedforward filters (FCF) or mathematical morphological filters[16] (MMF) can then be used to monitor the CVT transient information as shown in Fig. 23

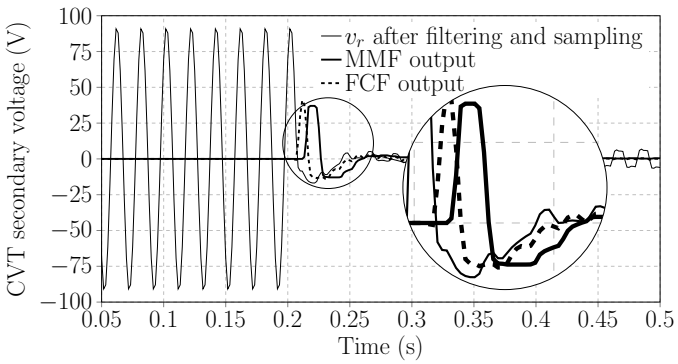

Fig. 23. Extracted CVT transient information using MMF and FCF

This filtered information V_{rf}, V_{yf}, V_{bf}(Fig. 24) can be monitored against lower and upper threholds (V_{lth}, V_{uth}) to adapt the time delays.

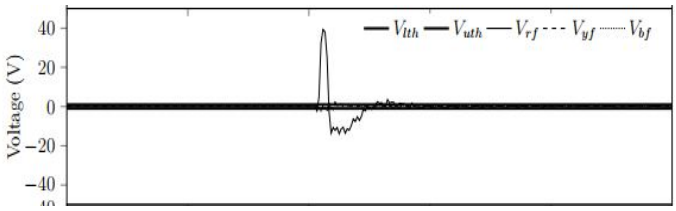

Fig. 24. Extracted CVT transient information

2) SIR Detection: One of the major factors influencing the CVT transients is SIR. This SIR is detected using the memorized information and based on the estimated SIR (Fig. 25), the time delay is made adaptive. Often, this is handled by manufactures for active type CVTs.

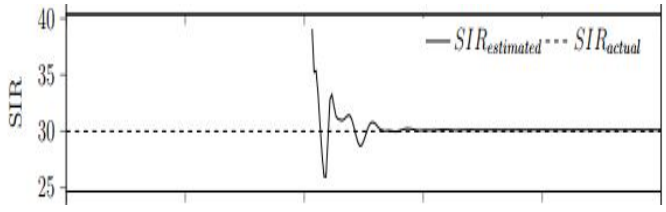

Fig. 25. Estimated SIR

3) CVT Transient Detection Logic [17]: This patented technique involves CVT transient detection logic which relies on undervoltage and overcurrent element to declare an CVT transient condition i.e. low voltage without high current. The detection of this condition triggers a timer which delays the zone 1 operation for 1.375 cycles which is typically enough for the transient to die out. However, during a close-in fault with high SIR condition, zone 1 tripping should not be delayed and this is done by monitoring the smoothness of fault impedance

(m value) which is achieved using a variable threshold along the line length as shown in Fig. 26. Once the estimated fault impedance is smoothened, the timer is bypassed indicating a close-in fault and trip signal is released.

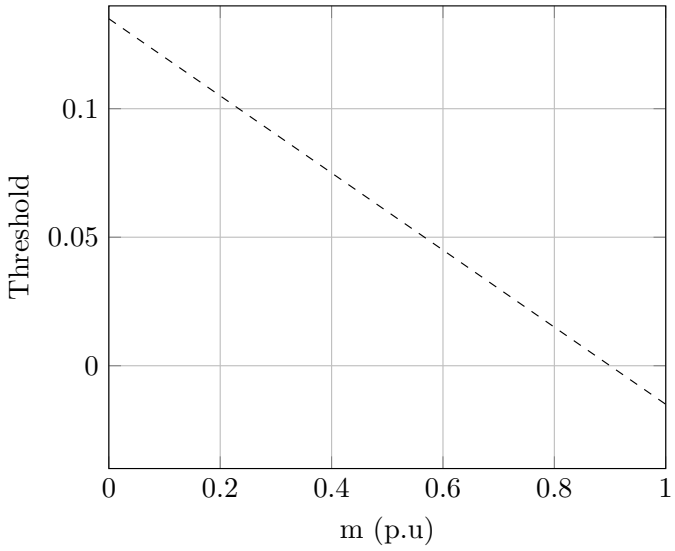

Fig. 26. Variable threshold to detect m value smoothness

This logic is enabled only when,

- the CVT is of active type
- CVT transient condition is detected
- when the SIR is greater than 5

D. Patentened CVT Filter [18],[19]

This patented filter is a two stage filter which is used in the voltage path to filter out the CVT transients. Equation 3 is the first stage filter which is designed to suppress decaying dc and oscillatory components at frequencies lower than the power system frequency.

$$v_{1(k)} = \sum_{n=0}^{20} h_n v_{(k-n)} \tag{3}$$

$$v_{2(k)} = \sum_{n=0}^{74} g_n v_1(k-n) \tag{4}$$

Equation 4 is for the second stage filter which provides dynamic memory and averages the information.
Equation 5 shows the combined filter whose filter coefficients (b_n) are shown in Fig. 27

$$v_{2(k)} = \sum_{n=0}^{94} b_n v_{(k-n)} \tag{5}$$

The key highlights of this filters are,

- The filter is designed to be universal and it does not require coefficient tuning for a particular CVT type i.e. active or passive
- The filter is designed to provide minimal time delay

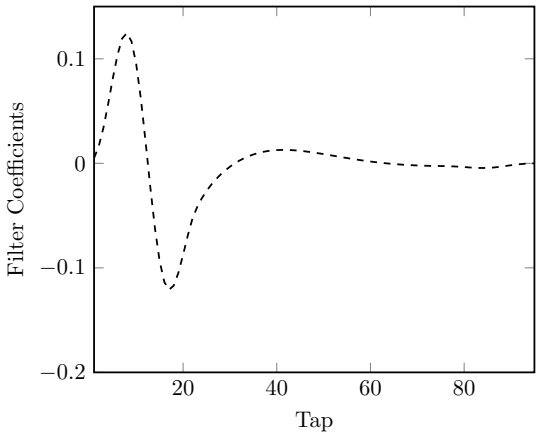

Fig. 27. Filter coefficients plot

Fig. 29 shows the performance of patented filter for a fault with active type CVT shown in Fig. 28.

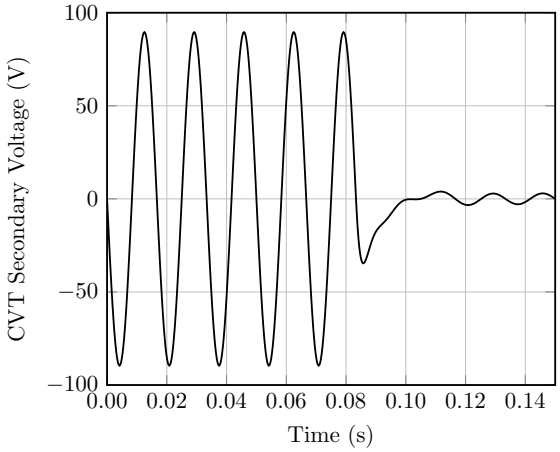

Fig. 28. CVT response - Active type

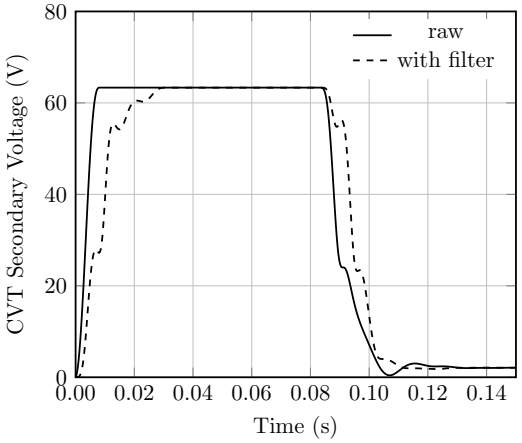

Fig. 29. Performance of patented filter

VI. Summary

- Ferro resonant suppression circuit cannot be avoided in CVT, as it is difficult to precisely predict and prevent ferro-resonant oscillation.
- Passive type CVT provides faster recovery time when compared to Active type CVT
- Passive type CVT has better transient response compared to Active type CVT
- In the case of active type CVT, the user has following options,
  1) To delay the tripping based on the estimated SIR
  2) Patented CVT filter to remove the transient information upfront before transformation with minimal time delay
  3) Patented CVT transient detection logic to adaptively delay the tripping
- In the case of passive type CVT, the user has following options,
  1) Patented CVT filter to remove the transient information upfront before transformation with minimal time delay

Appendix A
Coefficients of derived transfer function

$$
\begin{aligned}
N_3 &= L' L'_{TC} R'_{TC} C' \\
N_2 &= R_{TL} R'_{TC} L'_{TC} C' \\
D_5 &= L' L'_{TC} R'_{TC} C'_T L'_C C' \\
D_4 &= R_{TL} R'_{TC} L'_{TC} C'_T L'_C C' \\
&\quad + L' L'_{TC} L'_C C' + L' L'_{TC} R'_{TC} C'_T R'_C C' \\
D_3 &= L' L'_{TC} R'_{TC} C'_T + R_{TL} L'_{TC} L'_C C' \\
&\quad + L' R'_{TC} L'_C C' + R'_{TC} L'_{TC} L'_C C' \\
&\quad + R_{TL} R'_{TC} L'_{TC} C'_T R'_C C' \\
&\quad + L' L'_{TC} R'_C C' \\
D_2 &= R_{TL} R'_{TC} L'_{TC} C'_T + L' L'_{TC} \\
&\quad + R'_{TC} R_{TL} L'_C C' + R_{TL} L'_{TC} R'_C C' + L' R'_{TC} R'_C C' \\
&\quad + R'_{TC} L'_{TC} R'_C C' + R_{TL} R'_{TC} L'_{TC} C' \\
D_1 &= R_{TL} L'_{TC} + L' R'_{TC} + R'_{TC} L'_{TC} + R'_C C' R'_{TC} R_{TL} \\
D_0 &= R'_{TC} R_{TL}
\end{aligned}
$$

where,

$$
\begin{aligned}
L' &= L'_{T1} + L_{T2} \\
R_{TL} &= R'_B \\
R' &= R'_{T1} + R_{T2} \\
R'_B &= \frac{R_B \times FSC}{R_B + FSC} \\
C' &= C'_{eq} \\
C_{eq} &= C_1 + C_2
\end{aligned}
$$

$C'_{eq}, L'_C, R'_C, C'_T, R'_{TC}, L'_{TC}, L'_{T1}, R'_{T1}$ are the parameters of CVT referred to secondary of the intermediate step down transformer.

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