CT Saturation - A Simulation Study of Different Detection and Blocking Algorithms

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Why handling busbar CT saturation is critical

- Substation bus supplies large area and many customers
- Security and stability are most important
- Substation busbar has connections to multiple sources that feed fault
- Fault current can be very large, with severe CT saturation
Operational requirements for Busbar protection

- The security and stability of busbar protection are of paramount importance
- Fastest possible internal faults clearance time to minimize equipment damage
- High selectivity, a differential relay does not need to have any intentional delay to coordinate with relays in adjacent zones.
- Ability to operate fast if fault evolves from external to internal (breaker flashover).
The problem – CT saturation

When exciting voltage is greater than CT knee point
  • CT enters saturated region
  • Exciting current is large

Slows tripping / unsecure tripping
The problem – CT saturation

- AC and DC components in primary fault current
- Burden
- Remanence

CT type and construction
- CT characteristics, magnetizing curve, knee-point voltage
- Magnetic cores: smaller size—but susceptible to saturation
- Air cores: less saturation—but larger size
CT saturation detecting and blocking algorithms

- First: detect saturation....then apply
- Detecting from waveform (sinewave-shape) recognition - Method A
- Detecting from differential locus trajectory in the Differential-Restraint plane – Method B
- Release blocking if fault evolves into internal
Method A
CT saturation detecting and blocking algorithms

Method A
CT saturation detecting and blocking algorithms

Method A

Biased Char

CT Sat Allow to Trip

Safety Count

Trip

Method A
CT saturation detecting and blocking algorithms

Method B

Assessing differential performance at low region and high region
CT saturation detecting and blocking algorithms

Method B

Low Region

CT Sat
Detected
&
Safety
Count
Trip

High Region

PCE
1
&
1

CT Sat
Detected
Method B

1
&
1
Safety
Count
Trip

High Region
Method B

Phase-comparison element (PCE) detects internal / external fault

DIR = 1
Internal fault: no current source is greater than 90-degrees apart

DIR = 0
External fault: one or more current sources are greater than 90-degrees apart
CT saturation detecting and blocking algorithms

Method B

Differential trajectory during CT saturation

- **t₀** – Fault inception
- **t₁** – Saturation-free time
- **t₂** – CT saturated

**External-fault CT saturation…do not trip!**
CT saturation detecting and blocking algorithms

Method B

Increasing restrain during CT saturation is another measure for security
Evaluation Methodology and Test Results

Busbar for evaluation testing

Diagram showing a busbar with CTs and transformers labeled as follows:
- BB1
  - 33kV/132kV 100MA
  - CT1
  - CT6
  - CT5
  - CT4
  - CT3
  - CT2

BB2
- 132kV/33kV 10MA
Evaluation Methodology and Test Results

Influencing factors

- Fault type (ph-G, ph-ph, ph-ph-G and 3-phase faults)
- Fault location
- Fault resistance (to 260 ohms)
- Fault-current level (to 20 p.u.)
- Fault-inception point on wave (0°, 45° and 90°)
- Time to saturate (1/8, 1/4 and 1/2 cycle)
- Load-current level
- Vary CT remanent flux and the secondary burden for different times to saturate (TTS) and saturation severity
Evaluation Methodology and Test Results

External faults

(a) Phase A fault currents from all terminals
(b) Phase A differential and bias currents
Evaluation Methodology and Test Results

External faults—Method A blocks CT saturation

- Method A blocks CT saturation
  - Inhibit pulses short differential current lobes

(a) Positive inhibit pulses

(b) Negative inhibit pulses

(c) Trip decision

(Stable, no trip)
Evaluation Methodology and Test Results

External faults—Method B fast detector involves PCE—ultimate security

(a) CT saturation detector output

(b) Phase comparison output

(No trip)

(c) Trip decision
Evaluation Methodology and Test Results

Internal faults - Deep saturation in 1/8 cycle can slow trip

Method A trips 10.8 ms after the fault inception. Method B trips in 3.3 ms.
Evaluation Methodology and Test Results

Evolving faults - must respond quickly and securely

(a) Phase A fault currents from all terminals

(b) Phase A differential and bias currents

The trip decisions are made at 23 ms and 29 ms, respectively, after the fault evolution
Conclusions

- Method A: waveform-recognition technique
- Method B: trajectory based of bias and differential currents method; paired with phase-comparison element (PCE)
- Both methods remain stable for all external faults
- High-level security is consistent with theories of operation
- Both respond promptly to evolving faults—Method A faster tripping time
- Both enhance busbar protection and can decrease CT requirements
- Methodology presented can be used to verify any other algorithms or relays.
Thank You

Questions?