CT Saturation - A Simulation Study of Different Detection and Blocking Algorithms

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***Abstract* - Asymmetrical saturation of conventional current transformers (CTs) during a through fault, where significant spurious differential current can be produced, is the biggest operating risk to a low-impedance differential scheme.**

Encouraging developments have been made in non-conventional CT technologies such as those based on Rogowski coils and optical sensors. However, until these are fully industrialized, protection relays must counter the impact of CT saturation.

The risk is further elevated for busbar protection, which experiences a large proportion of through faults and might encounter substantially greater current on the faulted feeder. Over the decades, busbar protection products have been in service, based upon different relay technologies ranging from static relays to numerical relays.

A static, busbar relay based on the use of analogue electronic devices detects CT is saturation by comparing phase current with a reference signal from an RC (resistor-capacitor) circuit that periodically charges and discharges the capacitor. Upon detection, the differential path is short-circuited for that portion of the cycle during which saturation occurs.

Numerical busbar relays use a phase-comparison element to supervise a bias characteristic, which improves protection stability during through faults. In the latest numerical busbar relays, the bias characteristic is divided into a low region and a high region. These regions are supervised by a directional element, or by an enhanced phase-comparison element, and a saturation detector. For a fault located in the low region, the differential protection operates only if the directional element confirms an internal fault. For a fault located in the high region, the differential protection operates on its own if no saturation is detected. If saturation is detected, the differential operates in the same manner as does the low region.

This paper analyzes different CT-saturation detection techniques, comparing advantages and disadvantages. Technique performance is evaluated in the Simulink environment by integrating these with a sample-based, bias-differential model. The models were tested extensively by applying COMTRADE test cases covering a wide range of scenarios. These scenarios included influencing factors such as fault type, fault location, fault resistance, fault inception angle, CT saturation time and duration, load-current level and composition, source strength, and fault-evolution time. The test results are discussed, with some interesting conclusions drawn.

I. INTRODUCTION

Conventional current transformers (CT), which are based on electromagnetic principles using a magnetic core, can experience magnetic saturation during a transient system fault. Excessive excitation current is drawn because the CT is operating beyond its designed linear range, and the secondary current becomes distorted and reduced as a result. Asymmetrical saturation of terminal CTs during a through fault is the biggest operating risk to a low-impedance, differential scheme. CTs on one or more terminals get saturated and significant spurious differential current can be produced. The risk is further elevated for busbar protection, which experiences a greater proportion of through faults than the protection of any other power system apparatus. Busbar protection encounters substantial high current on the faulted feeder because of multiple sources feeding into it, often without significant system impedance in between to limit currents.

Encouraging developments have been made in non-conventional CT technologies such as those based on Rogowski coils and optical sensors. However, until these are fully industrialized, protection relays must counter the impact of CT saturation. This papers analyses and evaluates different CT saturation detection and blocking techniques to ensure security and dependability for busbar protection.

II. OPERATIONAL REQUIREMENTS FOR BUSBAR PROTECTION

Although not fundamentally different from other system protection, busbars serve a critical role in supplying power to a large geographical area; this intensifies the emphasis put on essential requirements for security and speed [1].

The security and stability of busbar protection are of paramount importance. Busbar faults are rare, and this is especially true with modern air-insulated switchgear (AIS) / gas insulated switchgear (GIS). In fact, a large proportion of them result from human error rather than the failure of switchgear components. With a typical fault rate of no more than one fault per busbar in 20 years, the installation of busbar protection might increase the level of disturbance to the power system; it is important to provide stable protection.

Accidental mis-operation of busbar protection might cause widespread disruptions because of the large number of feeders (and hence customers) affected.

Unit busbar protection must be highly dependable during internal faults. Although rare, the damage resulting from any uncleared fault can be very extensive, resulting in widespread system disturbances and equipment failures. Damage could even cause the complete loss of a station by fire, because of the large number of short-circuit current contributing sources [2]. High-speed busbar protection is required to limit the damaging effect on equipment and system stability, and to maintain service to as much load as possible. High dependability is also critical for faults evolving from external to internal, as a result of circuit breaker flashover, for example.

Typically, utilities apply differential protection for the busbar as the main protection because of its high selectivity. With high selectivity, a differential relay does not need to have any intentional delay to coordinate with relays in adjacent zones. Thus, differential protection provides high-speed operation [2].

Most modern busbar protection schemes use the biased (sometimes called "percentage-restrained") [1][2], low-impedance, differential protection technique. This method is popular because of its ease of application. Also, it offers advantages of high sensitivity at low current levels and high stability at high current levels, at the same time. The unique emphasis of busbar protection requirements on security and speed, however, has meant that CT saturation can be a particularly challenging problem for busbar protection. Any CT saturation counter measures can slow down operation for internal faults.

III. THE PROBLEM – CT SATURATION

Busbar differential protection is particularly vulnerable to CT saturation, with severe consequences if unmanaged.

A CT is like any other kind of transformer; it consists of two windings magnetically coupled by the flux in a saturable steel core. A time varying voltage applied to one winding produces magnetic flux in the core, which induces the voltage in the second winding to deliver the secondary current [3][4]. The transformer draws an exciting current to keep the core magnetized [5]. In practice, because of copper losses, core losses, eddy-current losses and leakage flux, the secondary current of a CT is not a perfectly true replica of the primary current. The errors between the primary and secondary currents are

far more prominent during power system transients such as system faults.

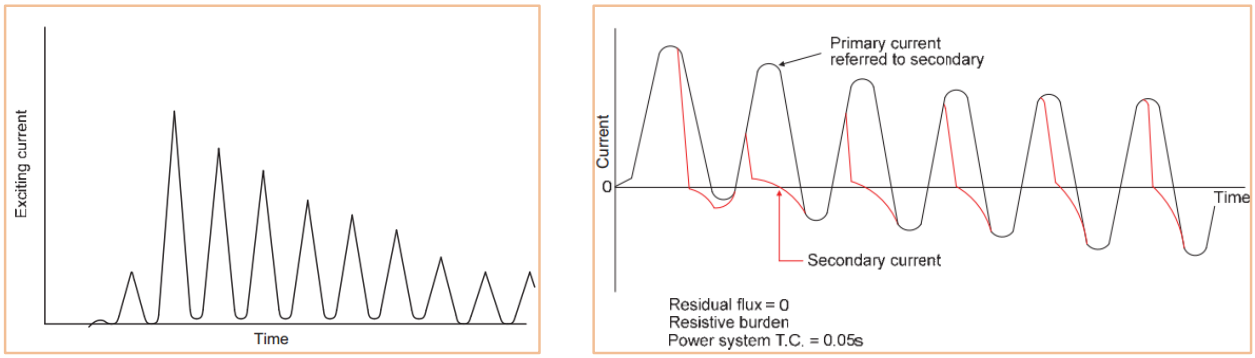
When the exciting voltage is greater than the knee point in the magnetizing curve, the CT enters the saturated region, in which the exciting current is no longer negligible. The secondary current becomes distorted and is no longer sinusoidal. When saturation is caused by symmetrical current with no DC offset, it is referred to as AC saturation. When the saturation is caused by DC component in the fault current, it is referred to as DC saturation. Saturation is likely a combination of both, as seen in typical power system fault current. The DC component builds up the mean flux over a period corresponding to several cycles of the AC component; during this period the AC component produces a flux swing about the varying 'mean value' established by the DC component. The asymmetric flux ceases to increase when the exciting current is equal to the total asymmetric input current; beyond this point the output current, and hence the voltage drop across the burden resistance, is negative. When the exponential component drives the CT into saturation, the magnetizing inductance decreases, causing a large increase in the alternating component in the exciting current. Figure 1 shows a typical exciting current during the transient period and the corresponding resultant distortion in the secondary current output because of saturation. It is apparent that significant spurious differential currents will be produced during a through fault if some, but not all, of the CTs involved in a differential scheme are saturated, or if all the CTs are saturated to varying extents.

The AC and DC components are driven by the primary fault current, which cause AC and DC saturations in the secondary current. These two are obvious influencing factors of the saturation severity. Other influencing factors include the secondary CT burden, the level of remanent flux, and the size and type of CT.

For a given CT and at a given primary current, the exciting voltage increases when the secondary CT burden increases. As a result, greater secondary burden increases the exciting current, which leads to increased likelihood and severity of CT saturation.

Remanent flux is the magnetic flux that is retained in the magnetic circuit after the fault current has been removed; this occurs as a result of circuit breaker opening. When the CT is subjected to a subsequent primary fault current, the flux will start from the remanent value, which may act to push the core into deeper saturation within shorter time if the instantaneous flux has the same initial direction as the remanent flux.

CTs with a solid core, such as Class TPX CTs [6], are relatively small. Because of its high magnetic-flux density, these are susceptible to saturation from a large remanent-flux level. CTs with air gap, such as Class TPZ CTs, are less seriously saturated but are relatively large.



(a) (b)

Figure 1. Typical exciting current (a) and distortion in secondary current (b) because of saturation

IV. CT SATURATION DETECTING AND BLOCKING ALGORITHMS

Over the last decades, busbar-protection products have been in service based upon different relay technologies ranging from static relays to numerical relays. These products used different CT-saturation detection techniques. A few examples of the theories of operation are described as follows.

A static busbar relay, which is based on the use of analogue electronic devices, detects when a CT is saturated by comparing phase current with a reference signal generated by an RC circuit that periodically charges and discharges a capacitor [7]. Upon detection, the differential path is short-circuited for that portion of the cycle during which saturation occurs. This method is referred to as Method A in this paper for convenience.

In a numeric busbar relay, the biased characteristic is divided into a low region and a high region which are supervised by a phase comparison element (PCE) and a saturation detector [8]. The PCE also operates a settings-free contributor calculation that ensures only terminal currents of genuine significance are involved in the PCE criterion. For a fault located in the low region, the differential operates only if the PCE confirms an internal fault. For a fault located in the high region, the differential operates on its own, if no saturation is detected. If saturation is detected, the differential operates in the same way as the low region. This method is referred to as Method B.

Another solution uses a 'phase comparison' element to supervise a bias characteristic, to improve protection stability during through faults [9].

Other algorithms include one based on rate of change of the currents flowing in and out of the protected zone [10]. Another involves a smoothing filter for the bias (restraint) current [11].

Method A and Method B are studied in great details by modelling in the Simulink environment and integrated with a sample-based, bias differential algorithm [12]. The characteristic for this algorithm is shown in Figure 2, with its settings. A sampling rate of 24 samples per cycle is used in both models. Sample-based bias-differential algorithms are considered for the very fast operating times, which represent a large challenge for the ability of a CT-saturation detection method to maintain protection stability during through faults. If it is sufficiently fast and reliable for a sample-based differential algorithm, it will be sufficiently fast for those based on other techniques.

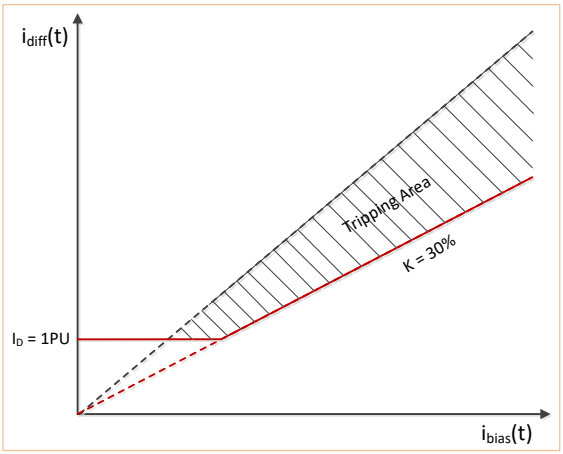


Figure 2 – A bias differential characteristic

A. Method A

Method A is a static busbar relay that uses analogue electronic devices. The principle used is to detect when a CT is saturated and to short circuit the differential path for that portion of the cycle during which saturation occurs. The resultant spill current does not then flow through the measuring circuit and stability is achieved.

The circuit shown in Figure 3 (a) and (b) has two electronic switches connected in parallel with the differential relay. These switches are closed for the portion of the cycle for which the adjacent CT is saturated. For the waveforms shown in Figure 3 (a), the inhibit pulses, produced by a circuit that detects CT saturation, operate the switches to remove much of the resultant differential current. The relay does not operate. In the case of an internal fault, as shown in Figure 3 (b), the differential current is in phase with the current from saturated CT; the inhibit pulses only remove an insignificant portion of the differential current. The relay operates. Relay operation is relatively unaffected.

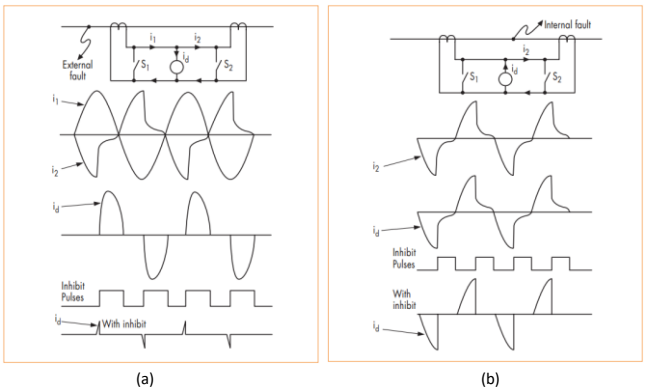


Figure 3 – Operating principle of a static low impedance busbar differential relay

These inhibit switches are easy to model in a numerical environment. The same inhibit can be achieved by gating the inhibit pulses with the differential current or the output of the bias-characteristics calculations; the latter is used in the paper.

Figure 4 shows the circuit for the saturation detector in a simplified form. A capacitor charges to the peak value of a DC voltage, V, that is rectified from, and proportionate to, the CT secondary current. A comparator evaluates V with half of the voltage stored in the capacitor V_c. The comparator produces the inhibit pulses when V is less than $0.5 \bullet V_c$. For an unsaturated waveform, the pulses produced at each zero crossing are of short duration. When the CT saturates, the waveform collapses earlier in the cycle and the pulse width increases.

In practice, inhibit pulses produced by negative portions of a zone phase-current waveform apply to positive portions of the zone's differential current waveform, and vice versa.

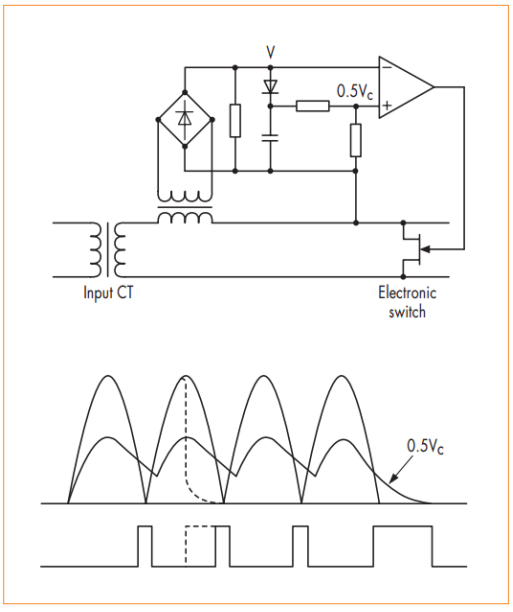


Figure 4 – Circuit for saturation detector

The RC circuit and the comparator are easy to model in the discrete domain. Capacitor voltage, V_c, is expressed by Equation 1, where k is the present sample index, ΔT is the sample interval, R is the discharge resistance and C is the capacitance.

$$\begin{cases} V_C(k) = |V(k)|, & if |V(k)| \geq V_C(k-1) \\ V_C(k) = V_C(k-1)e^{-\Delta T/RC}, & if |V(k)| < V_C(k-1) \end{cases}$$

Equation 1

Next, the CT saturation detection is gated with the bias characteristics to form the final trip decision, as shown in Figure 5.

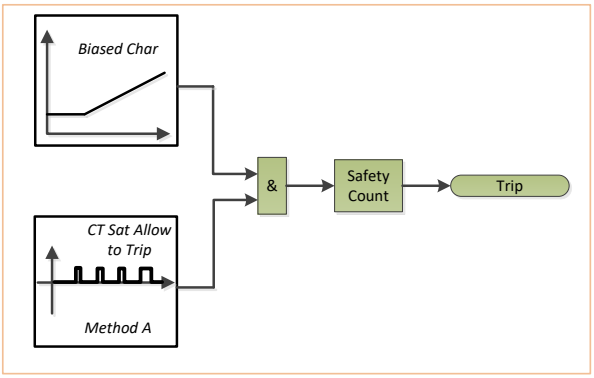


Figure 5 – Block diagram of Method A model

B. Method B

In Method B, the operating plane is divided into a low region and a high region. For a fault located in the low region, the differential operates only if the phase-comparison element (PCE) confirms an internal fault. CT saturations in this low region are unlikely and are difficult to detect. For a fault located in the high region, the differential operates on its own if no saturation is detected. If saturation is detected, the differential operates in the same way as the low region. Figure 6 shows the block diagram of this method.

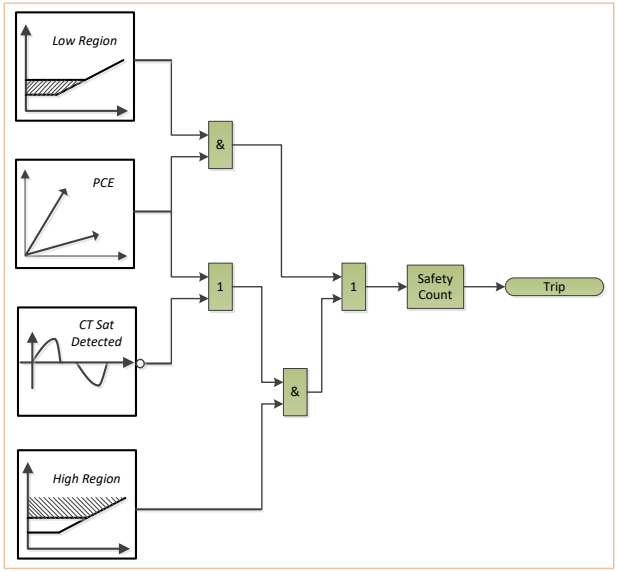


Figure 6 – Block diagram of Method B model

The CT-saturation detector consists of two elements: a slow and a fast detector. The slow detector checks if a bias current of large magnitude is accompanied by a differential current of relatively small magnitude; this indicates possible slow-occurring saturation.

The fast detector is an application of the time-difference method, as reported in ref [13]. It detects whether the bias current occurs before the differential current. This is based on the notion that CTs take time to saturate, so the spurious differential current produced because of CT saturation during an external fault develops after the fault inception. However, the bias current rises immediately. Figure 7 shows the time relationships.

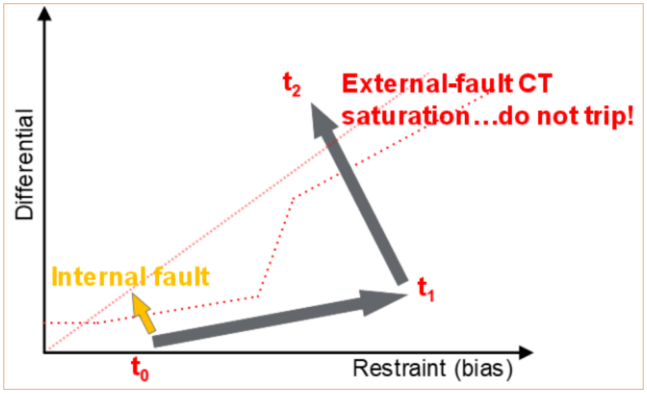


Figure 7 – Time-based CT saturation detection

The time between the two, which is the time to saturate, can be very short. It can be as quick as 1/8 of a cycle in the most unfavourable conditions such as a large fault current with large remanent flux. Therefore, sample-based algorithms are preferred for fast CT-saturation detection. Conversely, for an internal fault, both the bias and the differential currents rise at the same time as the fault inception, even when some or all CTs saturate.

The PCE module checks whether currents of significant magnitudes flow in one direction, which indicates an internal fault; or whether one of the currents flows in the opposite direction compared with the sum of the remaining currents, which indicates an external fault. Figure 8 shows the concept.

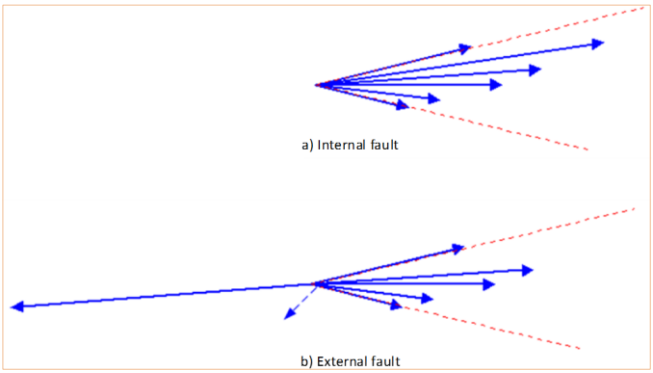


Figure 8 – Phase-comparison element detects internal / external fault

The PCE offers better selectivity by comparing a current with the sum of the remaining ones, than with the separate, remaining currents. The PCE is equipped with a settings-free contributor calculator that ensures only terminal currents of significant magnitudes are involved in the PCE calculation. Special measures are in place to cope with a saturated secondary current waveform characterized by large peak values and low RMS values. This paper uses a short-window Fourier transform of 1/8 cycle for phasor evaluation to better match the fast operate time of a sample-based differential algorithm.

V. EVALUATION METHODOLOGY AND TEST RESULTS

A simulation model of a 50-Hz, 132-kV system is configured using PSCAD/EMTDC, from which COMTRADE files are produced that contain the measured, CT secondary currents. The simulation system consists of two generators with one supplying the local busbar BB1 under study, through a 100-MVA transformer. The other generator is connected remotely through a 10-MVA transformer and an overhead line, as shown in Figure 9. The other four busbar feeders supply different load compositions with a combination of resistive, capacitive and inductive load. All CTs are ratio 1000/1 for easy calculation. The CT knee-points and secondary burdens vary to achieve different degrees of saturation.

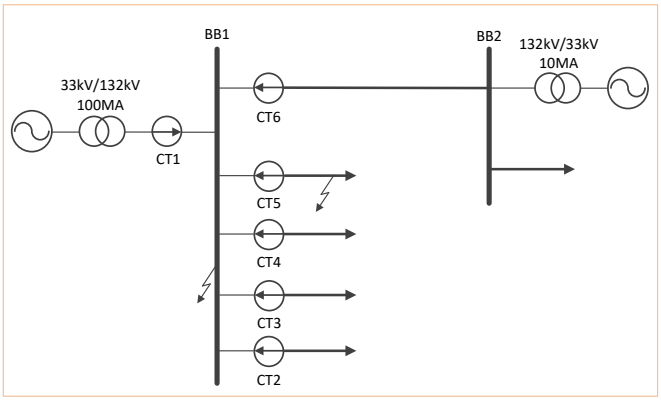


Figure 9 – A simulation power system

Many test cases were applied to Method A and Method B that cover a wide range of scenarios. Influencing factors were the following:

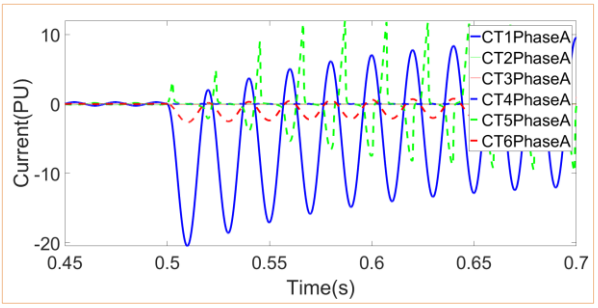
- Fault type (ph-G, ph-ph, ph-ph-G and 3-phase faults)
- Fault location
- Fault resistance (to 260 ohms)
- Fault current level (to 20 p.u.)
- Fault inception point on wave (0°, 45° and 90°)
- Time to saturate (1/8, 1/4 and 1/2 cycle)
- Load-current level

Different times to saturate (TTS) and saturation severity are achieved by varying the CT remanent flux and the secondary burden (also accounting for the fault-current level).

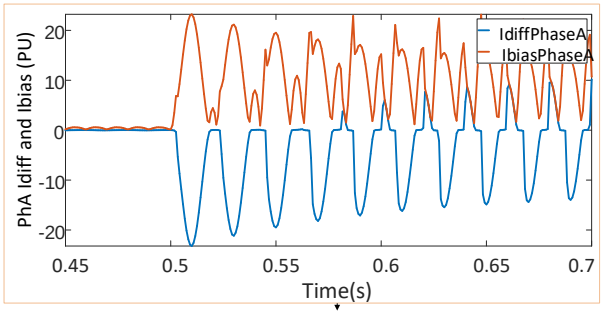
The interest areas for performance include protection stability during through faults, and operating time for internal faults and evolving faults.

A. External faults

Figure 10 shows the results for an external A-G fault occurring on Feeder 5 at the time of 0.5 s in which CT5 saturates within 1/8 cycle of the fault inception. This is a difficult case. Large-magnitude, spurious differential current

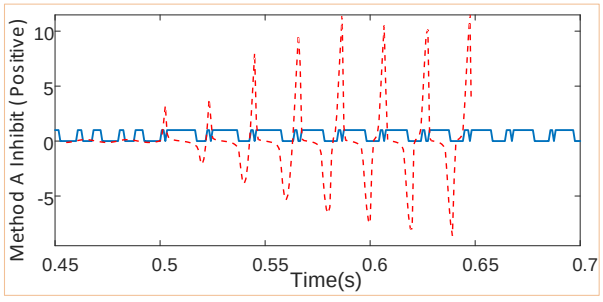


(a) Phase A fault currents from all terminals

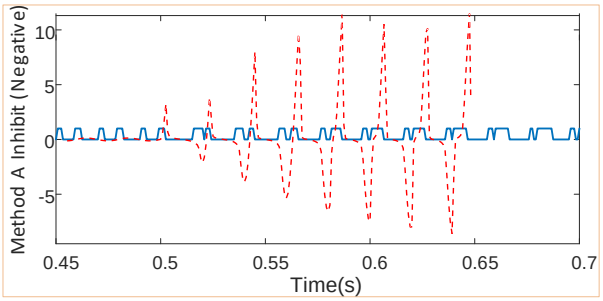


(b) Phase A differential and bias currents

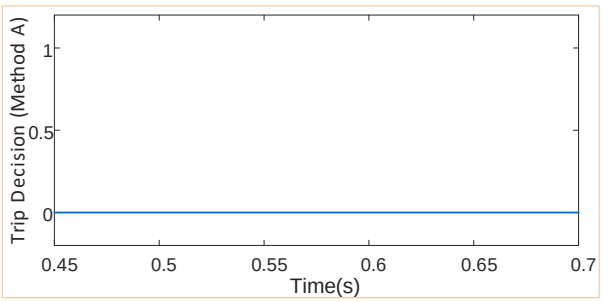
Figure 10 – An external A-G fault with a time to saturate of 1/8 cycle



(a) Positive inhibit pulses



(b) Negative inhibit pulses

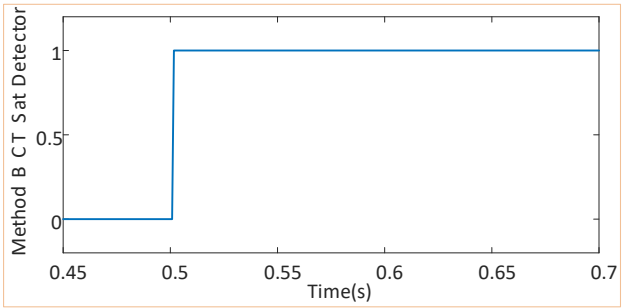


(c) Trip decision

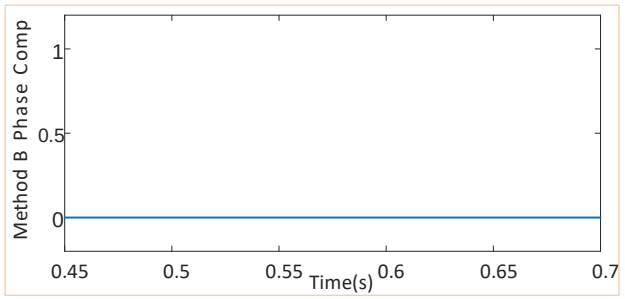
Figure 11 – Response of Method A to an external A-G fault with a time to saturate of 1/8 cycle

is produced per Figure 10(b) with one CT quickly and deeply saturated, and all the other CTs measuring linearly per Figure 10(a). Unless a fast and effective counter-saturation technique is in place, the sample-based, bias characteristic algorithm would mis-operate quickly.

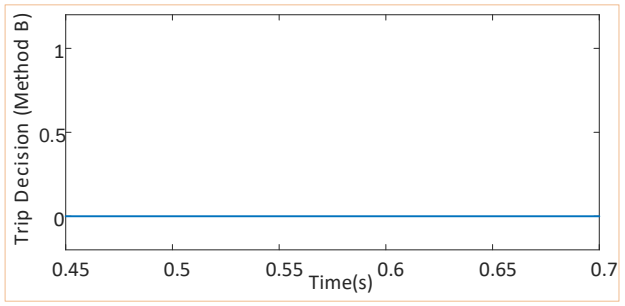
The Method A response is shown in Figure 11, where (a) and (b) show the positive and negative inhibit pulses, respectively. The positive inhibit pulses are of particular interest because the differential current in this case is of predominantly negative values. The wide inhibit pulses in Figure 11(a) are well positioned to coincide with the differential current lobes. Thus, the inhibit pulses short the differential current in a similar way as depicted in Figure 3 (a), ensuring that the trip decision remains stable throughout the fault, as shown in Figure 11(c).



(a) CT saturation detector output



(b) Phase comparison output



(c) Trip decision

Figure 12 – Response of Method B to an external A-G fault with a time to saturate of 1/8 cycle

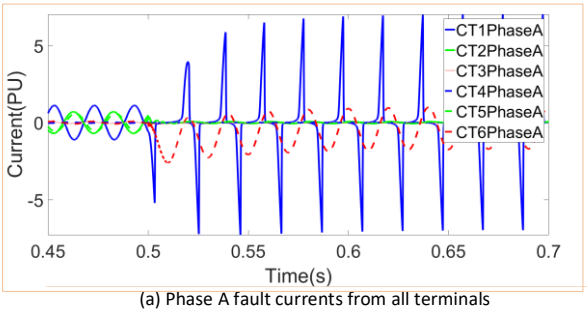
Alternatively, complete protection stability is also achieved by Method B, as shown in Figure 12, where (c) is the trip decision. Because of the large differential current, the fault is located in the high operating region and this requires the CT-saturation detector to decide whether to involve the phase comparison element (PCE). The fast detector detects successfully the small time difference between the starts of the bias and differential currents and decides that there is a possibly saturated CT during an external fault. The fast

detector makes the decision in this case as quickly as within 2 ms of fault inception, as shown Figure 12(a). The PCE produces a negative output as shown in Figure12(b), which guarantees protection stability.

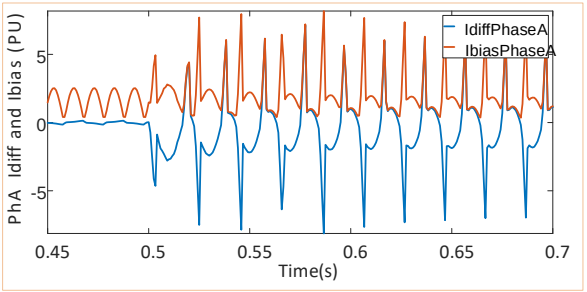
B. External faults

Often, during external faults, security of CT-saturation detection and blocking algorithms is achieved at the cost of slower operate times for internal faults. However, for high-speed, busbar protection schemes the algorithm operate time for an internal fault should be in the region of half a cycle or shorter.

Figure 13 is an internal A-G fault occurring at 0.5 s, in which CT1 saturates within 1/8 cycle of the fault inception. The challenge is that the CT on the feeder that provides the largest fault current goes into saturation rapidly and deeply (Figure 13 (a)). Thus, the differential current is reduced substantially (Figure 13 (b)) which slows down the protection trip.



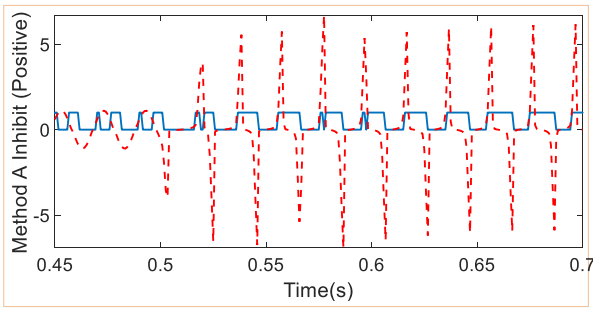
(a) Phase A fault currents from all terminals



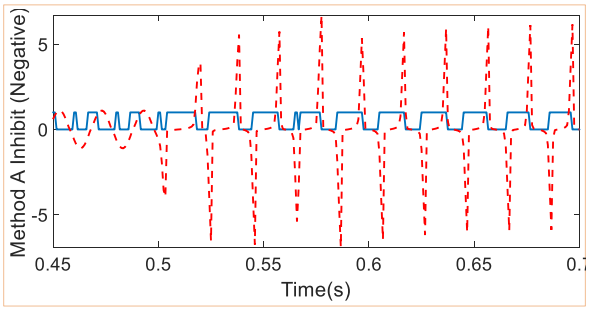
(b) Phase A differential and bias currents

Figure 13 – An internal A-G fault with a time to saturate of 1/8 cycle

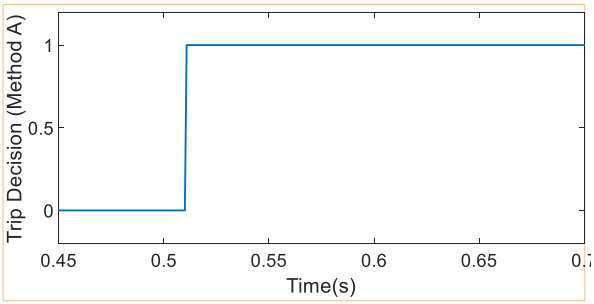
The Method A response is shown in Figure 14. The positive inhibit pulses of Method A are well positioned to avoid large portions of negative differential current and thus, allow the bias characteristic to operate. Similarly, in Figure 14(b), the negative inhibit pulses allow the portions of positive differential current to operate. Method A trips 10.8 ms after the fault inception.



(a) Positive inhibit pulses



(b) Negative inhibit pulses

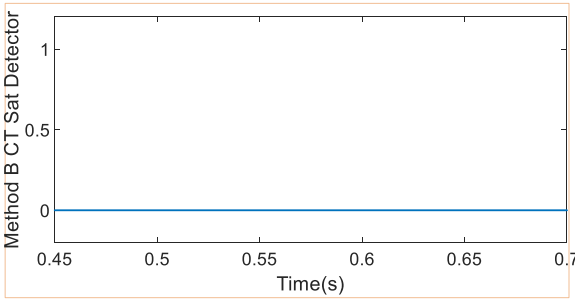


(c) Trip decision

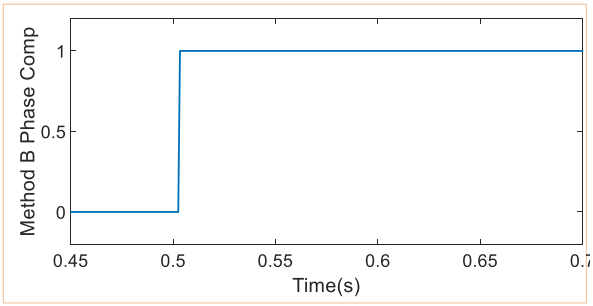
Figure 14 – Response of Method A to an internal A-G fault with a time to saturate of 1/8 cycle

For Method B, the reduced differential current takes the fault to the low operating region. This region requires the phase comparison element and the bias characteristic to agree, regardless of CT saturation, before the trip decision can be reached. Therefore, the output of the CT saturation detector, shown in Figure 15(a), is for indication only. Note that no saturation is detected anyway; this is an internal fault - the bias and differential currents occur at the same time. The phase comparison element gives a positive output 3.3 ms after the fault inception per Figure 15(b), with the trip decision issued at the same time per Figure 15(c).

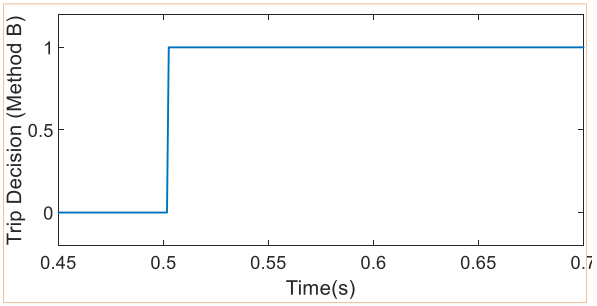
Both methods trip within the required time, with Method B tripping exceptionally fast.



(a) CT saturation detector output



(b) Phase comparison output



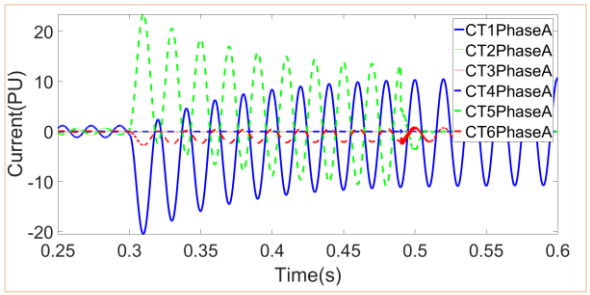
(c) Trip decision

Figure 15 – Response of Method B to an internal A-G fault with a time to saturate of 1/8 cycle

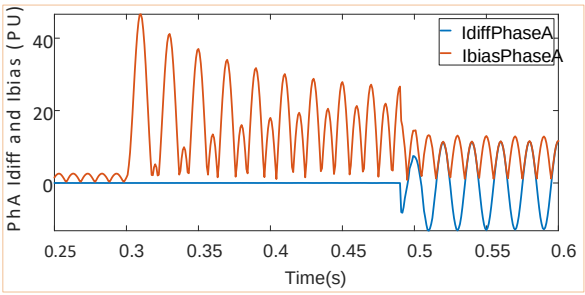
C. Evolving faults

A system fault can sometimes start at one location in the system before evolving to another location. Examples are circuit-breaker flashover or weakened insulation. When an external fault evolves into an internal fault, the protection scheme that was previously stable must respond promptly.

Figure ***16*** shows an external A-G fault, which occurs on Feeder 5 at 0.3 s, evolving into an internal A-B-G fault at the time of 0.49 s. No obvious CT saturation occurs in this case - the focus is on the speed of the transition in the internal logic of the algorithms. Both Method A and Method B detect successfully the evolved internal fault (see Figure 17 and Figure 18). The trip decisions are made at 23 ms and 29 ms, respectively, after the fault evolution.

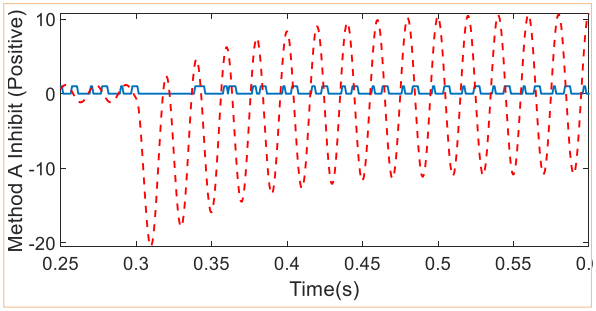


(a) Phase A fault currents from all terminals

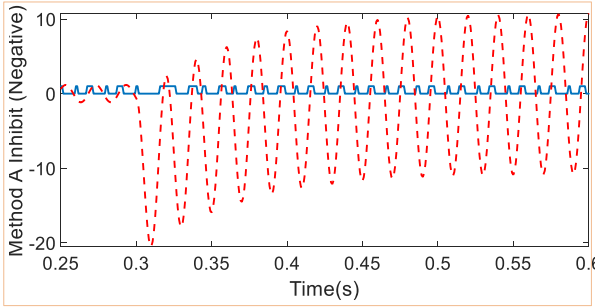


(b) Phase A differential and bias currents

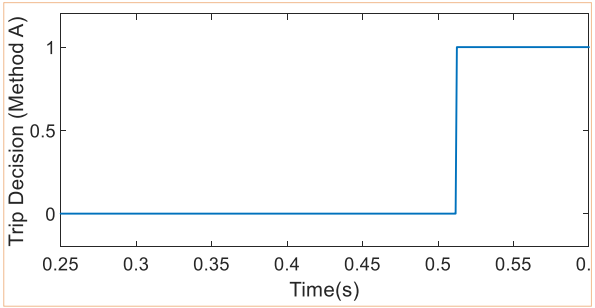
Figure 16 – An external A-G fault evolving to an internal A-B-G fault



(a) Positive inhibit pulses

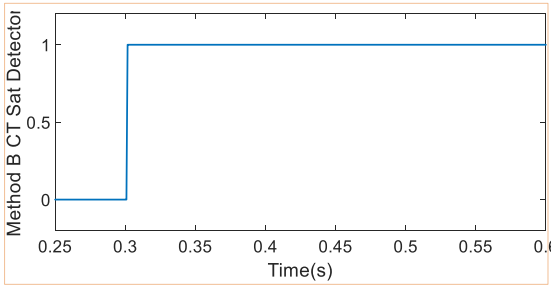


(b) Negative inhibit pulses

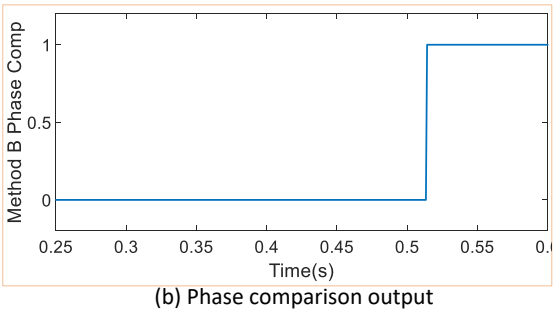


(c) Trip decision

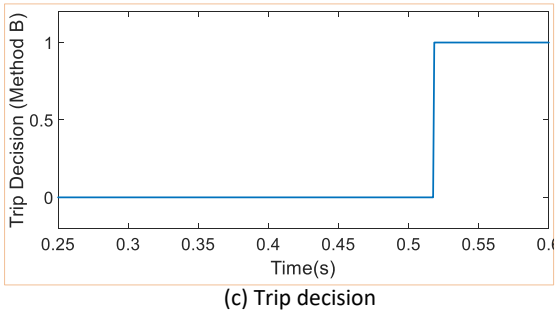
Figure 17 – Response of Method A to an external A-G fault evolving to an internal A-B-G fault



(a) CT saturation detector output



(b) Phase comparison output



(c) Trip decision

Figure 18 – Response of Method B to an external A-G fault evolving to an internal A-B-G fault

D. Results Summary

Both Method A and Method B demonstrate very good performance in the studies, with the results summarized in Table 1.

- Both methods remain stable for all external faults. This high-level security is consistent with the theories of operation
- Both methods achieve algorithmic operate times of near a half-cycle. Method B demonstrates exceptionally fast operation, with a sub-1/4 cycle trip time for all internal faults with a fault resistance of 80 ohms and less, and a sub-1/2 cycle trip time for all other internal faults
- Both methods respond promptly to evolving faults, with Method A providing a faster tripping time. This is because of its waveform-based technique that enables a near-instantaneous transition
- Method A has less calculation complexity. Therefore, it takes less processing bandwidth. However, both methods can be fitted easily and integrated into modern, intelligent electronic devices (IEDs)

	Method A	**Method B**
External faults security	Very high.	Very high.
Internal faults operate times	Fast. In the region of 1/2 cycle or less for faults with low fault resistances (< 50 ohms). Up to 1 cycle for faults with medium - high fault resistances (> 50 ohms).	Ultra-fast. Within 1/4 cycle for faults with low – medium fault resistances (< 80 ohms). Within 1/2 cycle for faults with high fault resistances (> 80 ohms).
Evolving faults operate times	Very fast. Within one and a half cycles for all evolving faults.	Fast. Within one and a half cycles for all evolving faults where the internal fault resistance is less than that of the external fault.
Product integration complexity	Easy.	Easy to medium.

Table 1 Summary of test results

The test cases covered a wide range of scenarios and influencing factors. Some of the cases, such as those described in A - C, are extremely challenging, with fast and severe saturation in some of the CTs. The authors expect that very few products can pass all the tests. For context, a typical numerical busbar differential relay with years of proven operations in the field was subjected to the tests of A and B. It failed for both cases. This makes the performance of Method A and Method B even more outstanding.

VI. CONCLUSIONS

CT saturation is a major operational risk to the protection security of a low-impedance differential protection scheme. The risk is heightened for busbar protection considering the very large impact of a mis-operation and the real likelihood of experiencing external faults with excessive fault currents from a large concentration of fault MVA.

This paper investigated two different techniques to detect CT saturation and supervise busbar bias differential protection. The first method, Method A, is based on a waveform-recognition technique first implemented in a static busbar relay with the use of analogue electronic devices. The other method, Method B, is based on detecting the time difference between the starts of the bias and the differential currents, along with employing a phase-comparison element.

The theories of operation of the two methods were explained and the results of a comprehensive simulation study, covering a wide range of influencing factors, were discussed in detail. The two methods were evaluated by integrating these with a sample-based, bias-differential characteristic and subjecting these methods to a series of internal, external and evolving fault cases. Both methods demonstrated satisfactory performance, with each strong in particular scenarios.

It is encouraging to note that different techniques can complement each other. These techniques can form the building blocks for future enhancements to improve the performance of busbar protection and drive down the CT requirements for busbar applications to handle the most stringent conditions of modern power networks.

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