# Determining CT Requirements for Generator and Transformer Protective Relays

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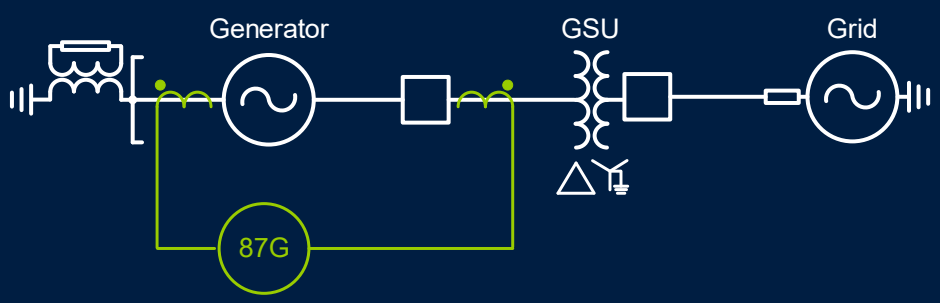
# Introduction



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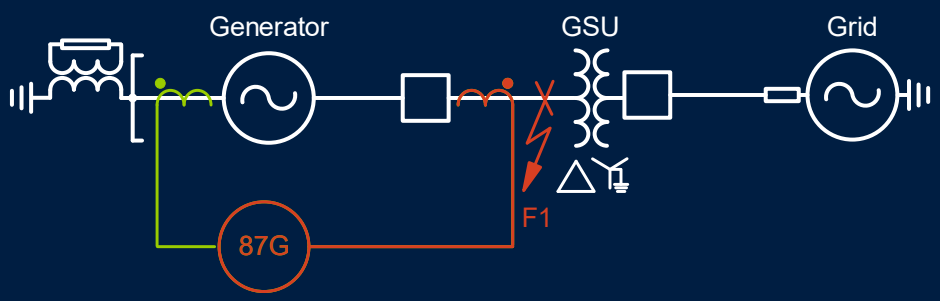


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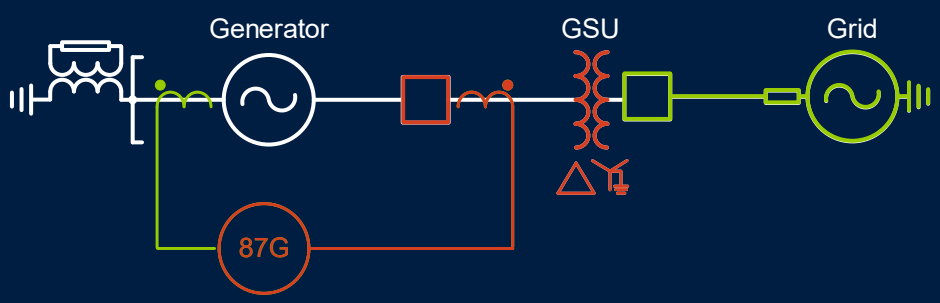

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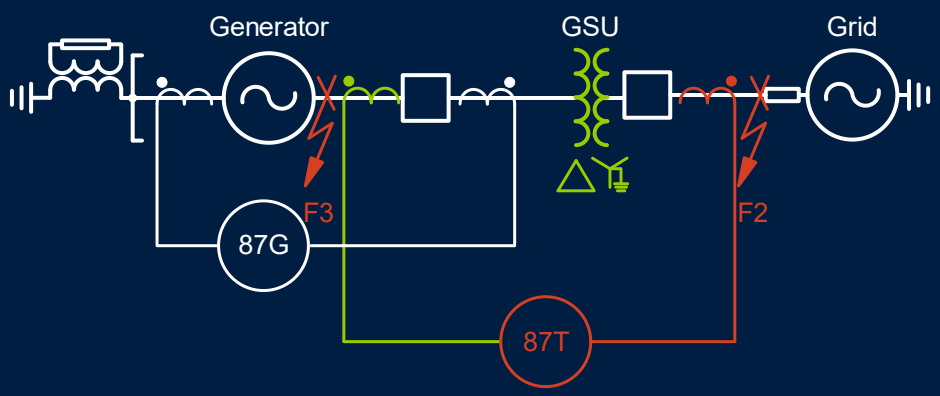


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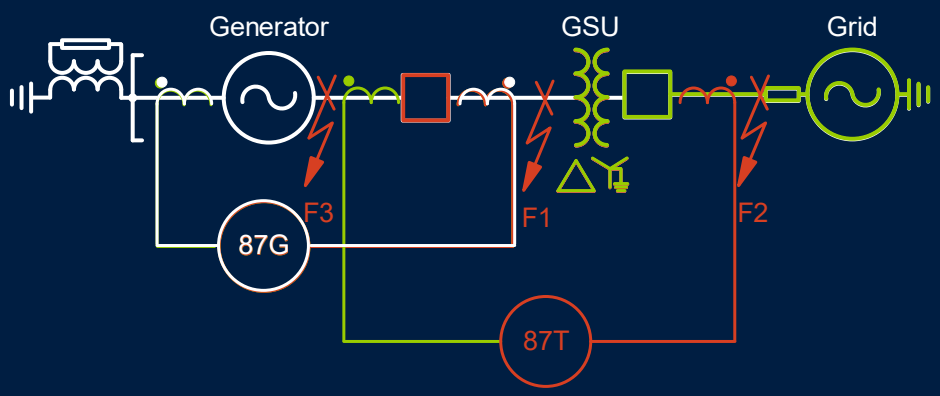

## Overview

- IEEE and IEC guidance
  - DC offset
  - Remanence
- CT models
- Differential relay scheme
- Test method and results
  - CT sizing
  - Relay settings

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  - Remanence
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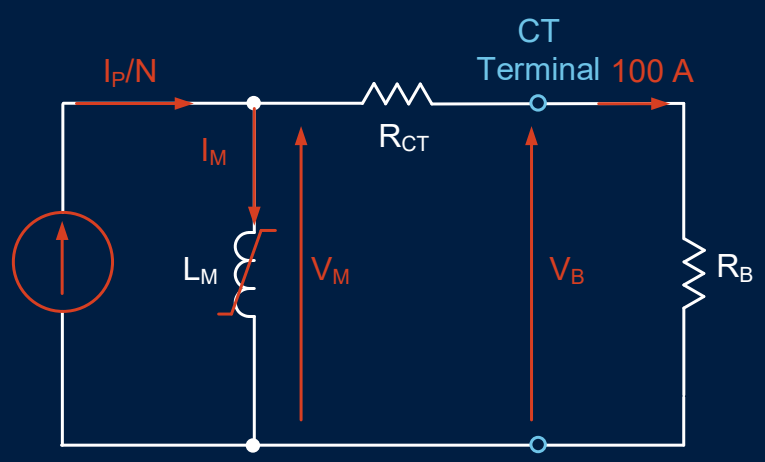
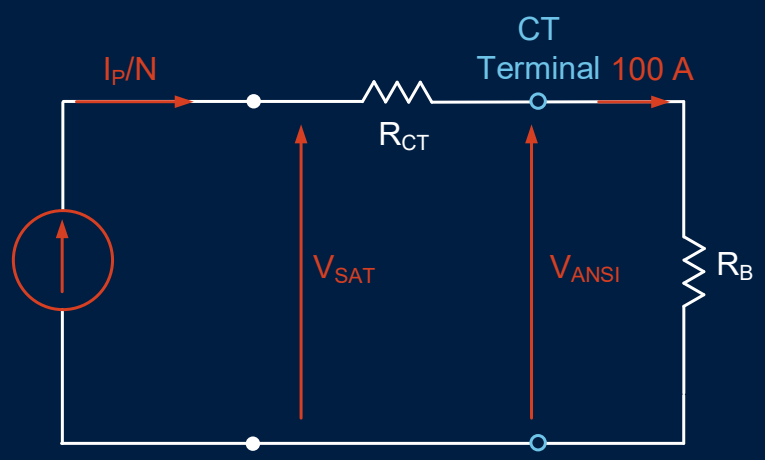
# IEEE and IEC Guidance

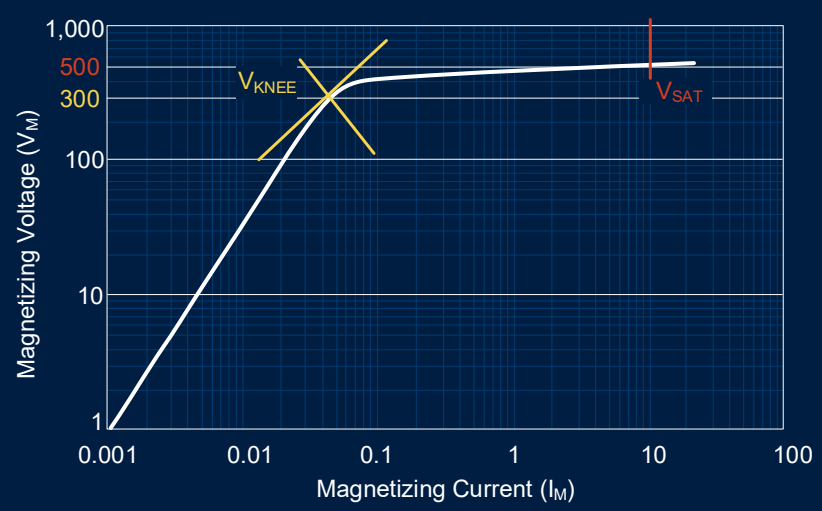
# CT Equivalent Circuit



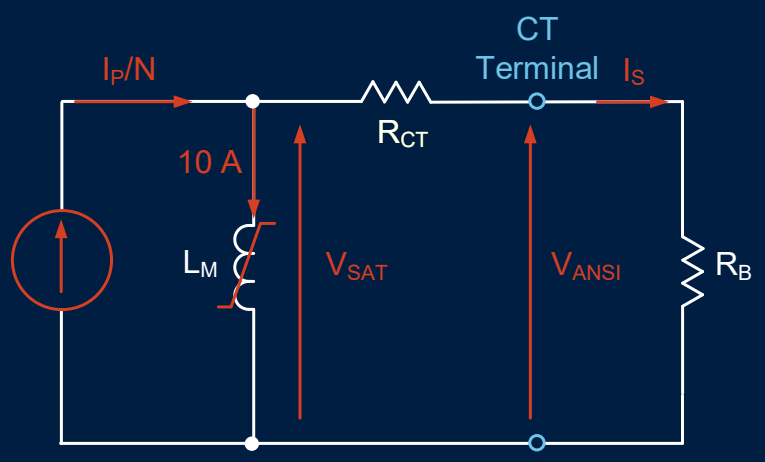
# CT Equivalent Circuit




# Saturation Voltage in Excitation Curve



# CT Equivalent Circuit

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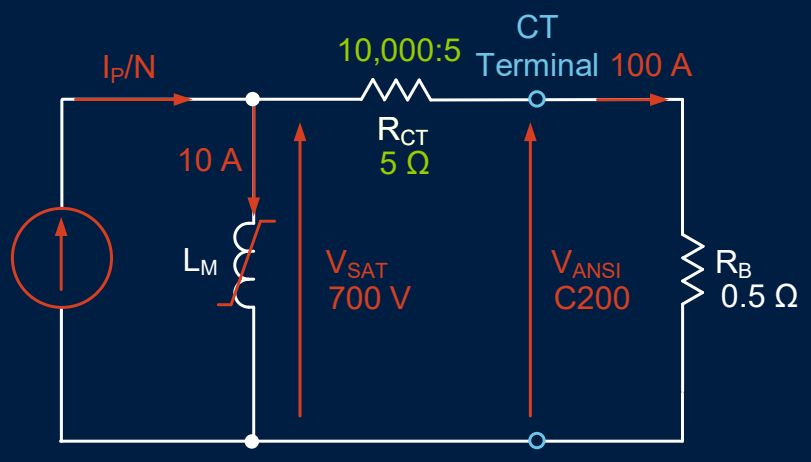
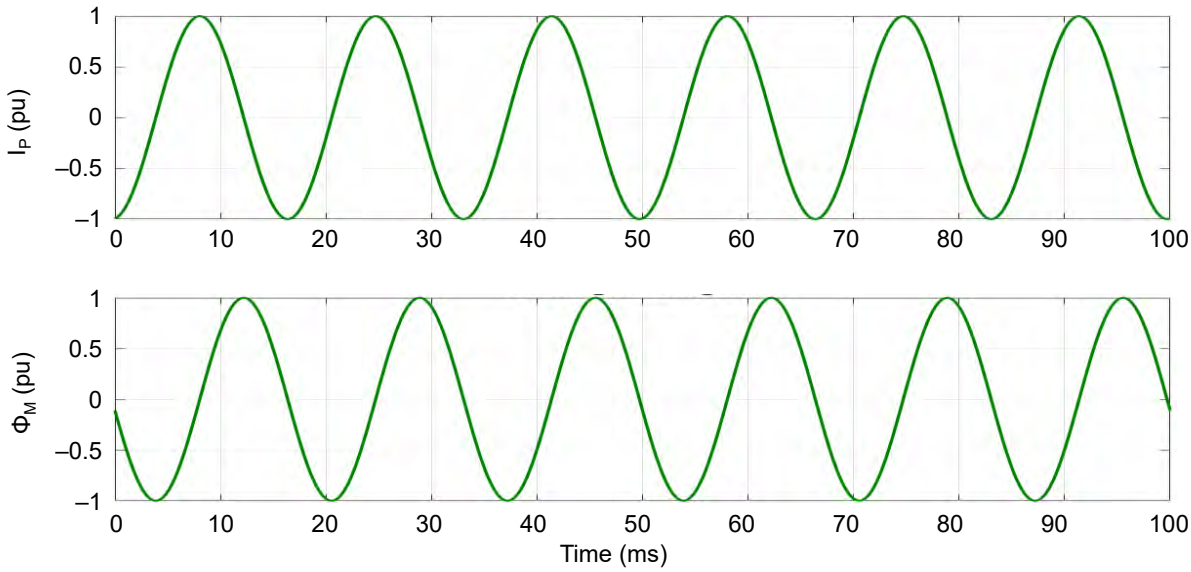


# Fault Current and CT Flux

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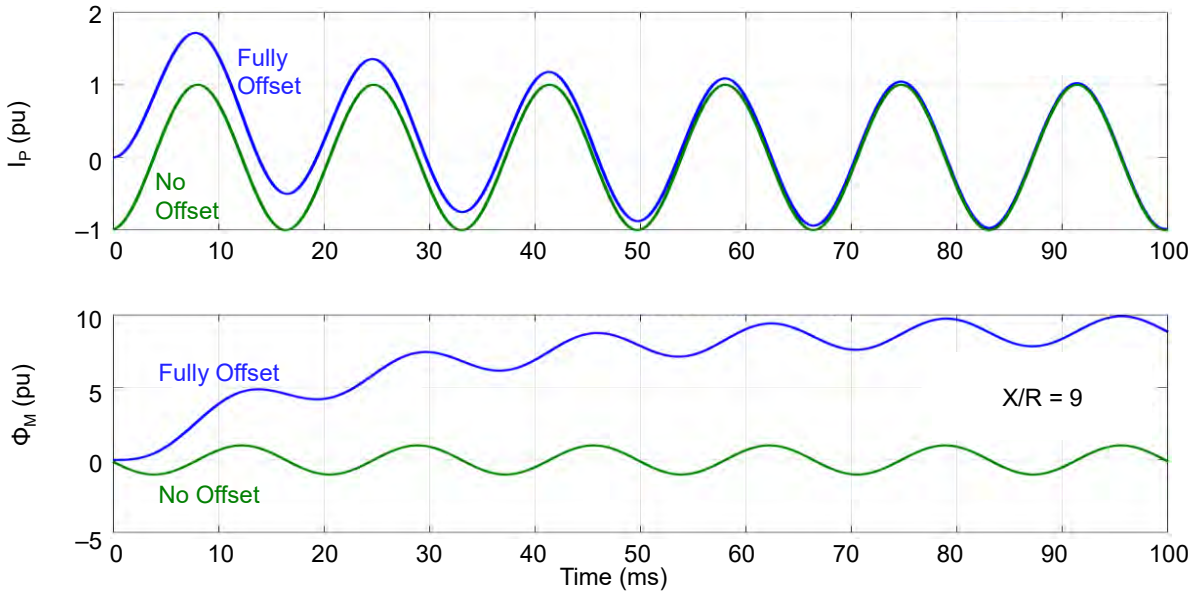

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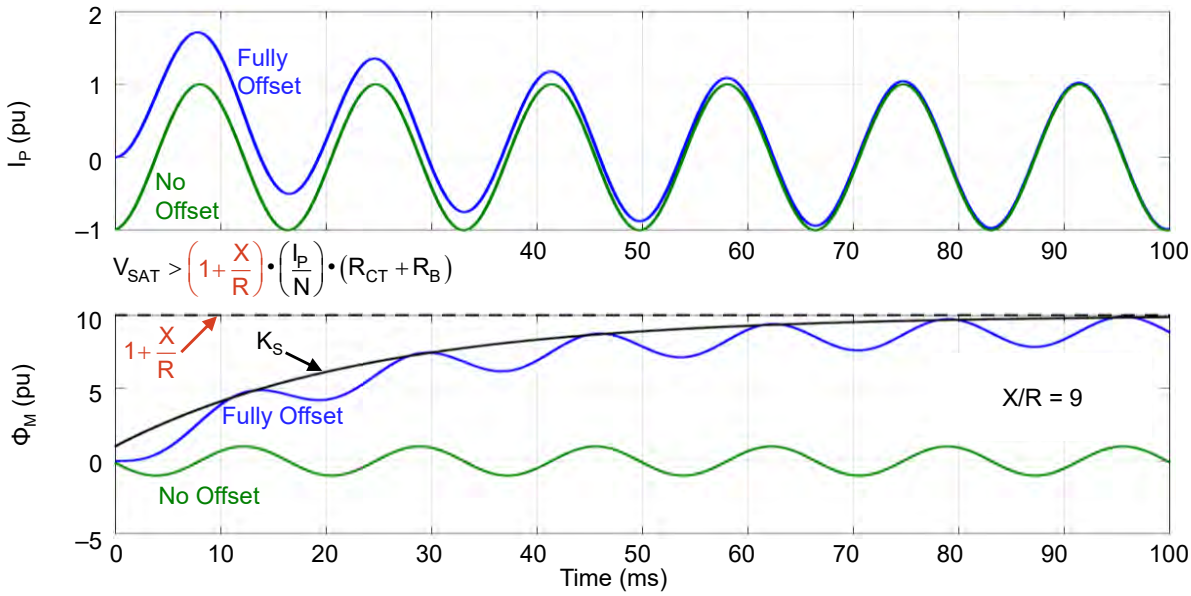
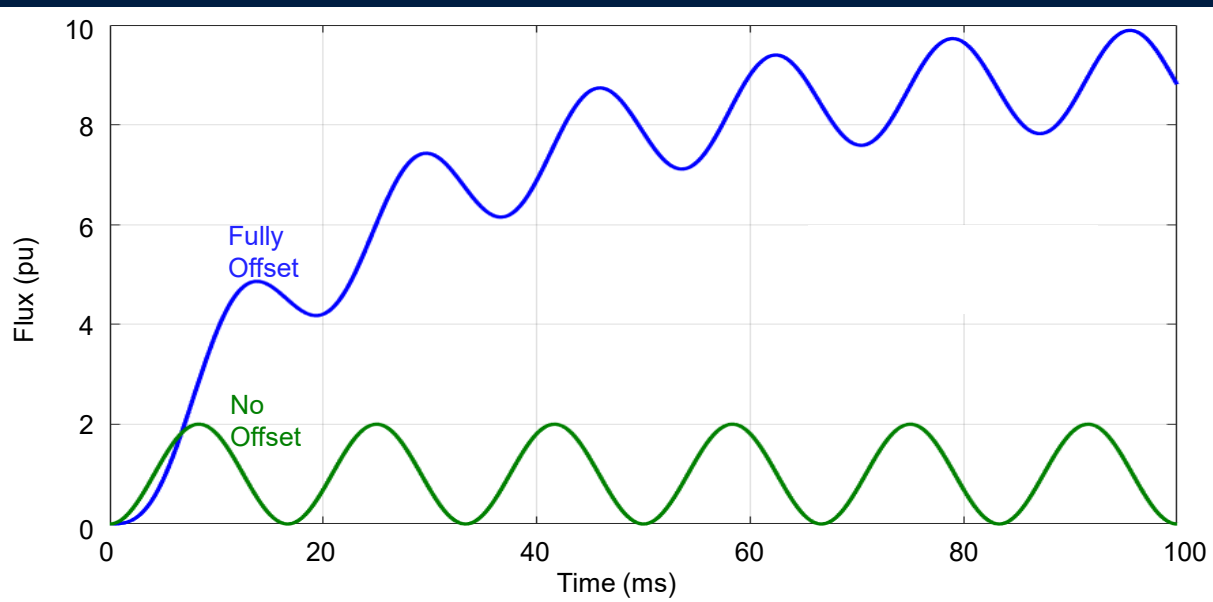



# Effect of Fault Inception Angle



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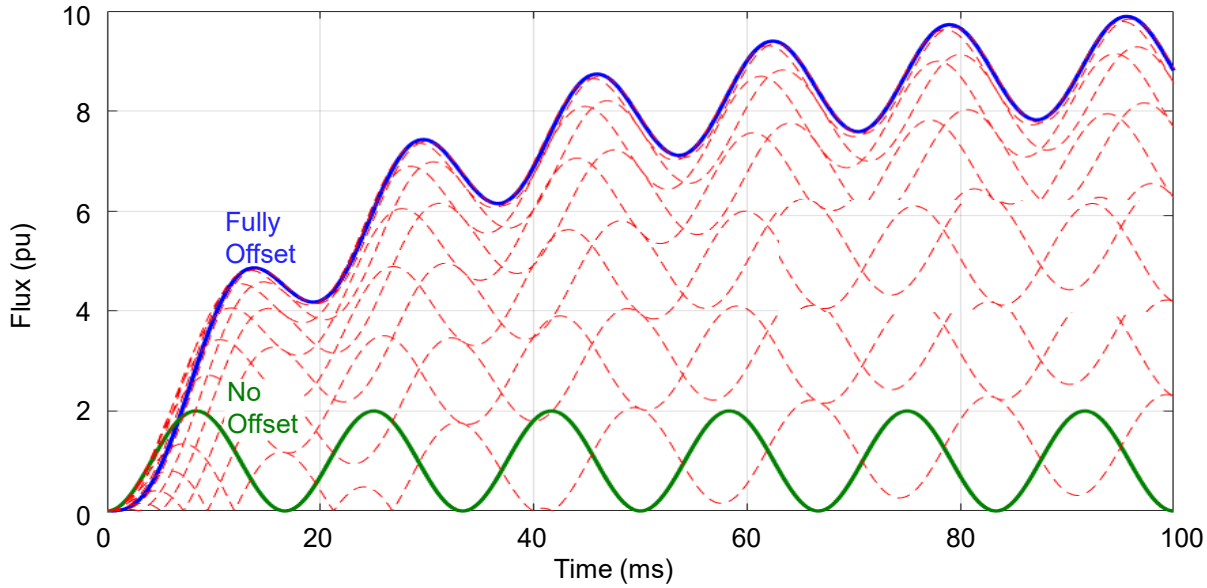
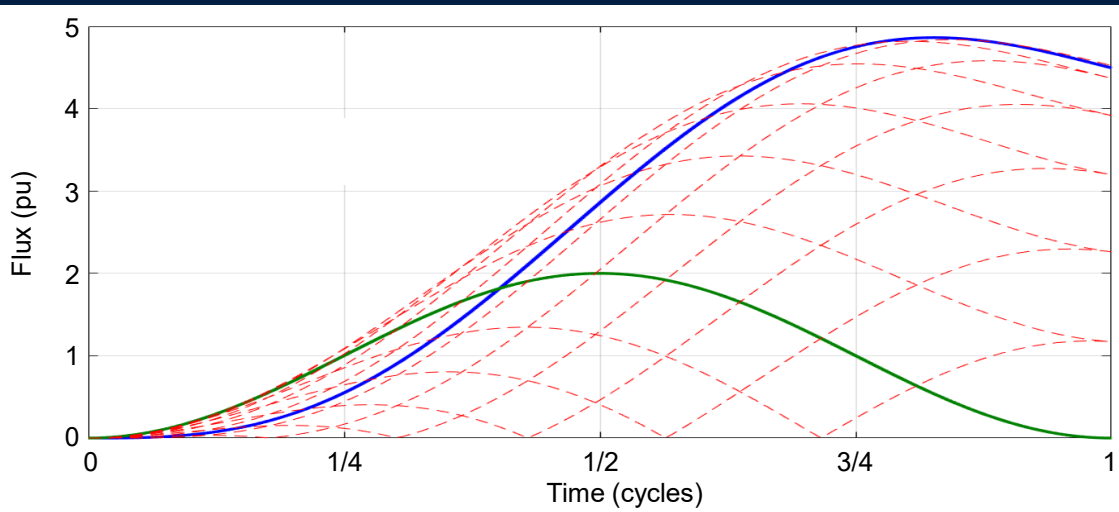



# Effect of Point-on-Wave




$$\underset{(IEC)}{K_{TD}} = \underset{(IEEE)}{K_S} = \frac{V_{SAT}}{I_S \bullet (R_{CT} + R_B)} \rightarrow V_{ANSI} = K_S \bullet I_S \bullet R_B$$

$$\rightarrow V_{SAT} = K_{TD} \bullet I_S \bullet (R_{CT} + R_B)$$

# Remanence

# CT Sizing

## DC Offset and Remanence

**IEEE**

$$V_{SAT} = \frac{\left(1+\frac{X}{R}\right)\cdot I_S\cdot(R_B+R_{CT})}{1-Rem}$$

DC and Relay  Remanence  Ohm's Law

**IEC**

$$E_{AL} = (K_{TD}\cdot K_{REM})\cdot I_S\cdot(R_B+R_{CT})$$

$$K_{REM} = \frac{1}{1-Rem}$$

# IEEE and IEC Surveys

## IEEE

| Remanent Flux | Percentage of CTs |
|---|---|
| 0–20 | 39 |
| 21–40 | 18 |
| 41–60 | 16 |
| 61–80 | 27 |

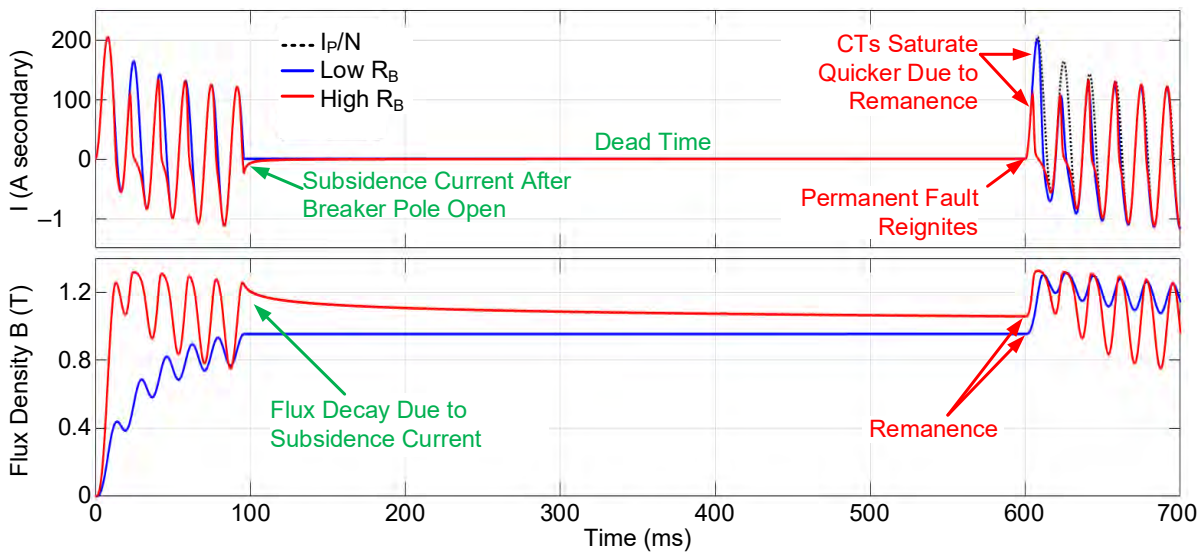
Remanent Flux Survey on 230 kV System

## IEC

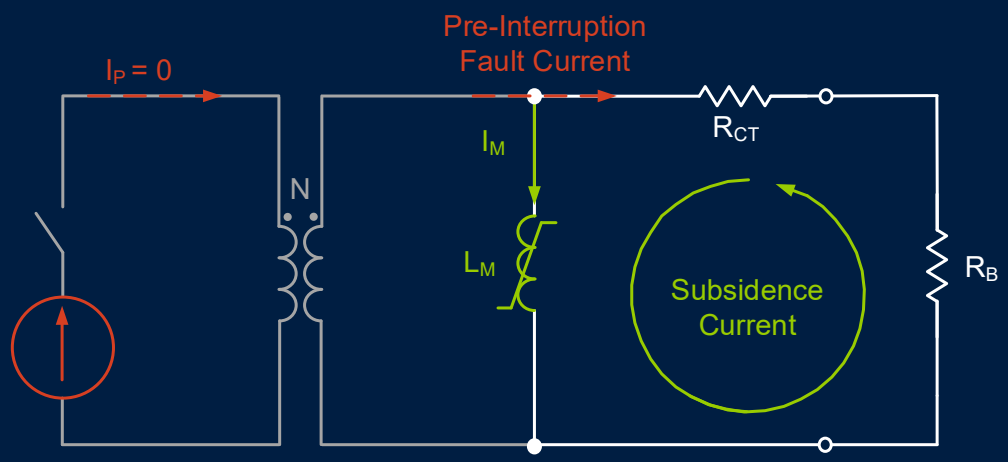
| | Old CT Cores | New CT Cores |
|---|---|---|
| **Theoretical Remanence** | 75–77% | 88–95% |
| **Measured Remanence** | 70–75% | 85–87% |

Theoretical and Measured Remanence

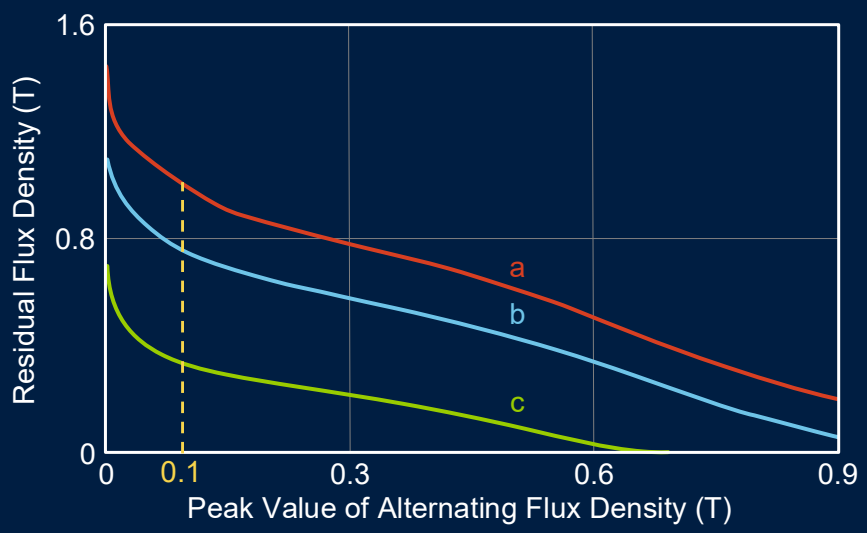
# Effect of Faults on Remanence



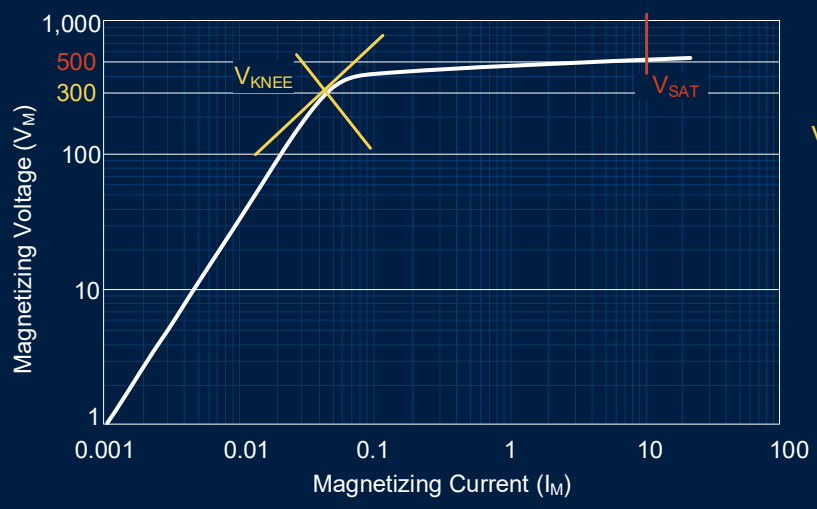
# Effect of Fault Current on Remanence




# Effect of Load

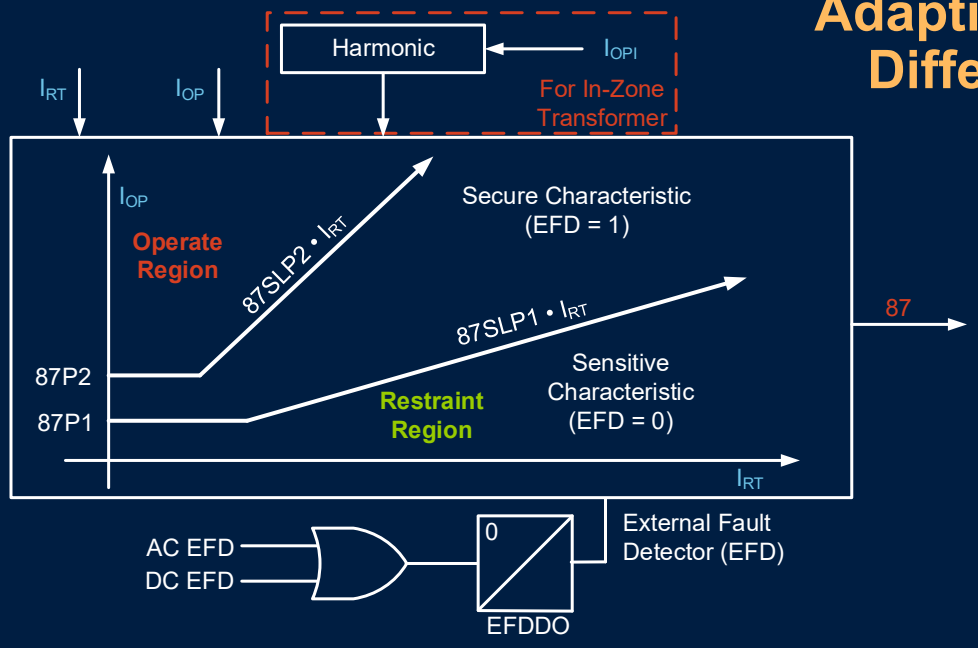


# Load and Excitation Curve

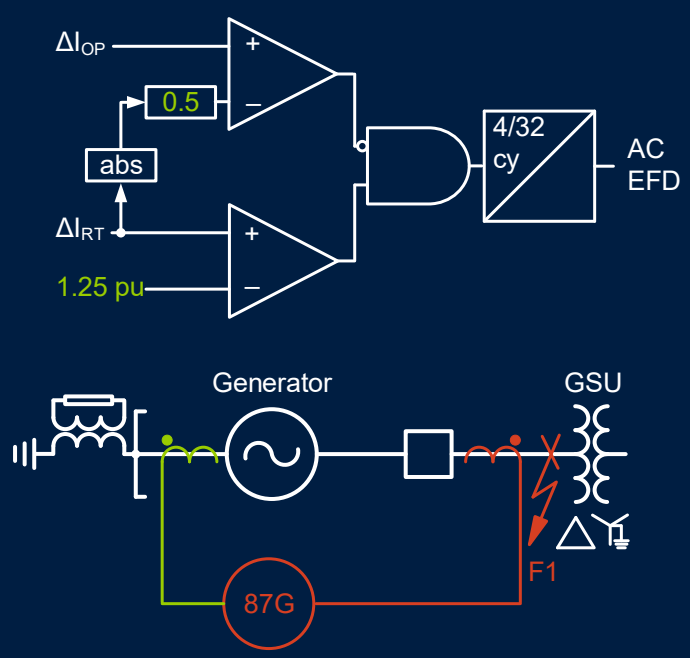


# Protective Relay Scheme

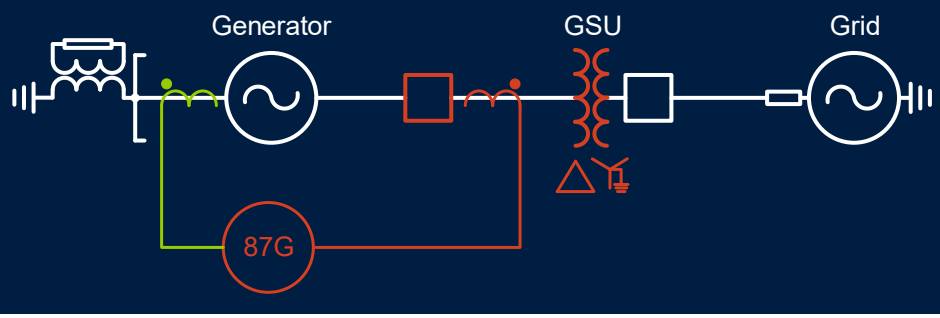
# Adaptive Slope Differential

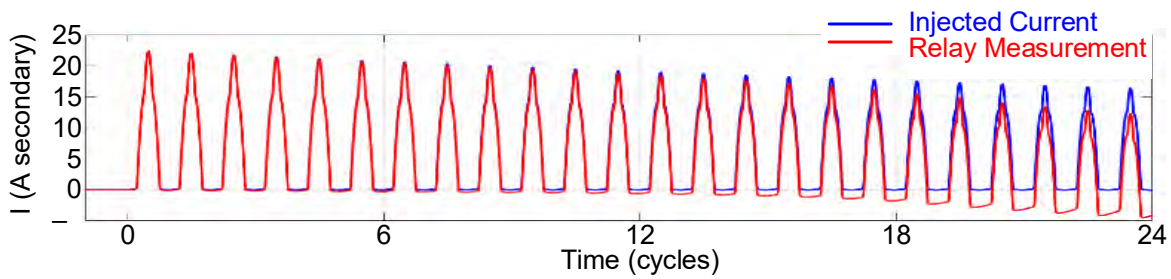



# External Fault Detector – AC EFD



# External Fault Detector – DC EFD

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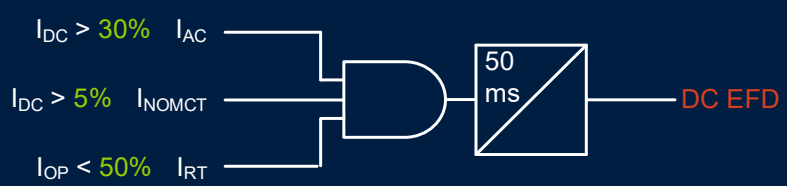
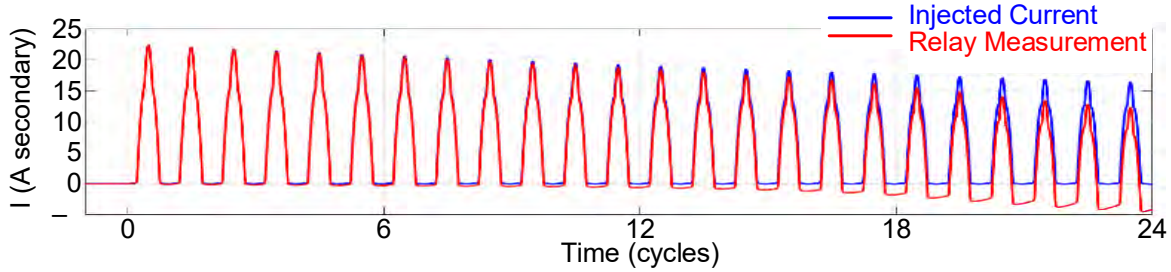
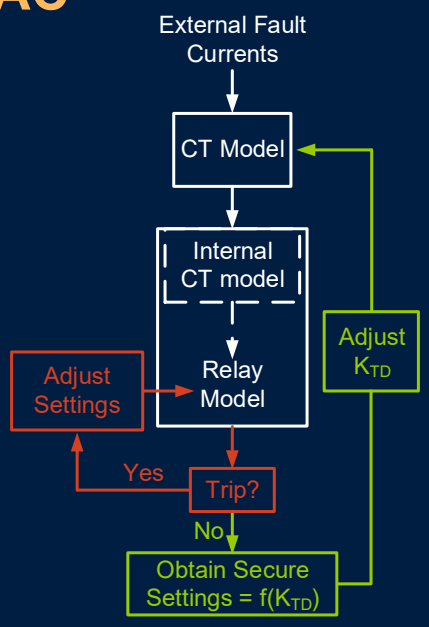


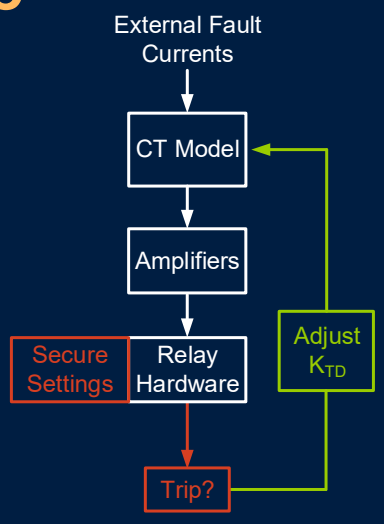
## Test Method – AC

- Point on wave (0 to 360)
- X/R: up to 100
- Both ground and phase
- One saturated CT, other not
- 87P1 and 87SLP1 set low
- Simulations with 5% margin

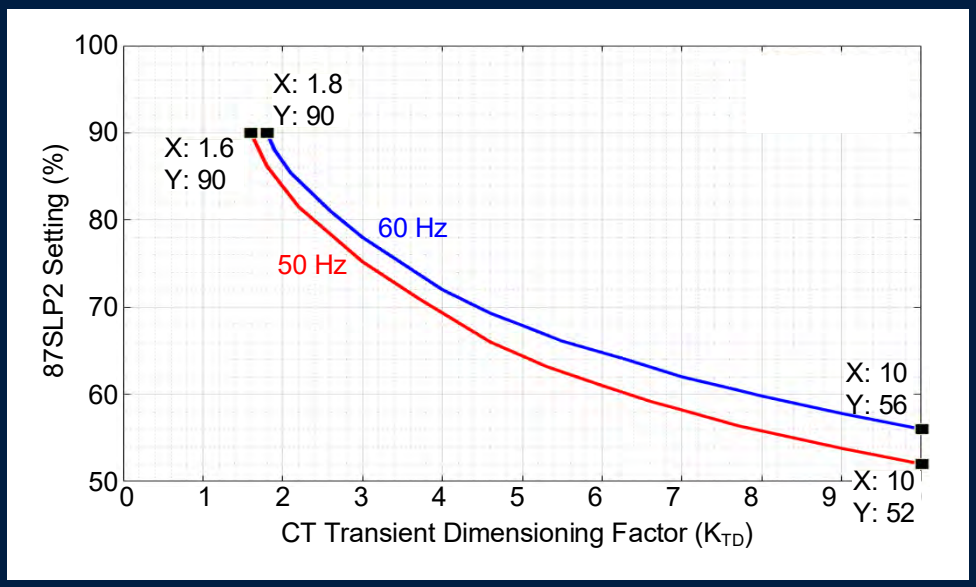



## Test Method – AC

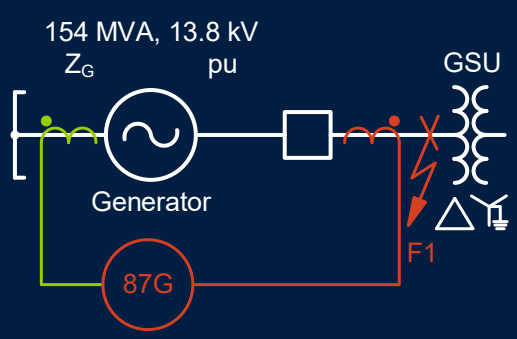
- Point on wave (0 to 360)
- X/R: up to 100
- Both ground and phase
- One saturated CT, other not
- 87P1 and 87SLP1 set low
- Simulations with 5% margin
- Hardware-in-the-loop verification



# CT Sizing Requirements and Relay Setting




# CT Sizing Requirement




$$V_{ANSI} = K_{REM} \cdot K_{S_MIN} \cdot \left(\frac{I_F}{N}\right) \cdot R_B$$

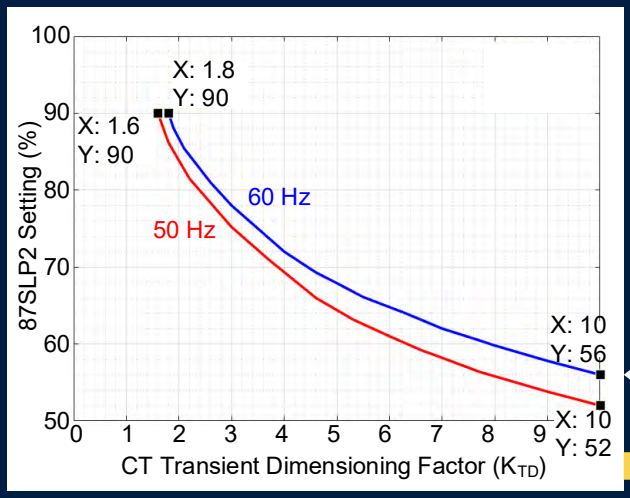
$$V_{ANSI} = 3 \cdot 1.8 \cdot \left(\frac{39{,}530\ A}{2{,}000}\right) \cdot \ .372\ \Omega = 39.7\ V$$

$$V_{SAT} = 3 \cdot 1.8 \cdot \left(\frac{39{,}530\ A}{2{,}000}\right) \cdot (\ .372\ \Omega + \ \ \Omega)$$

$$= 573.3\ V$$

$$V_{SAT_CT} = 1 \ \ V + 2 \ \cdot \ \ A \cdot \ \ \Omega = 6 \ \ V$$

# CT Sizing Requirements and Relay Setting

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$$V_{SAT} = 3 \bullet 1.8 \bullet \left(\frac{39{,}530\ A}{2{,}000}\right) \bullet (\ .372\ \Omega +\ \ \Omega)$$

$$= 573.3\ V$$

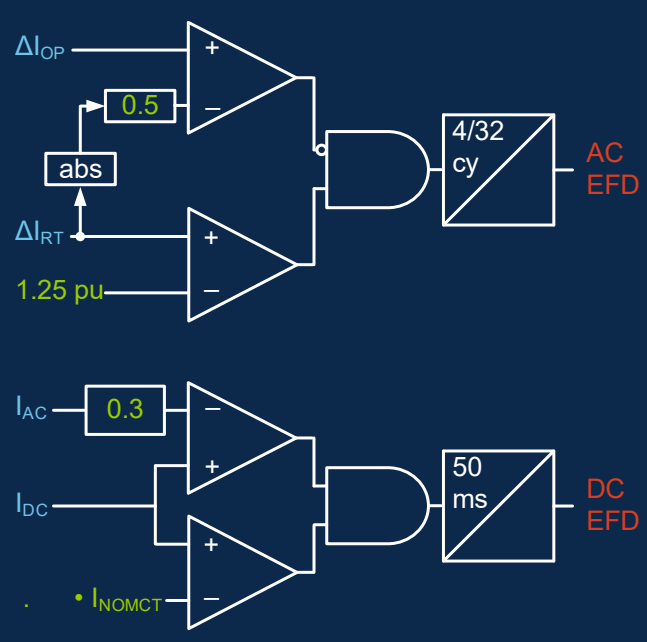
$$V_{SAT_CT} = 4\ \ \ V + 2\ \bullet\ \ A \bullet\ \ \Omega = 9\ \ \ V$$

$$K_{TD} = \left(\frac{900\ V}{573.3\ V}\right) \bullet 1.8 = 2.83$$

**87SLP2 = 79%**

# Test Method and Results – DC

- Down to a $K_S$ of 1
- Lower inrush
  - AC EFD drops out, but dc EFD does not
    87P2 = 0.50 pu
  - DC EFD drops out
    87P1 = .1 pu • $I_{nom}$/TAP
    ~ 0.25 pu



# CT Requirements Summary

# CT Size and Relay Setting

## Before → After

$$V_{SAT} = \left(1 + \frac{X}{R}\right) \cdot I_S \cdot (R_B + R_{CT})$$

$$V_{SAT} = 1 \quad \cdot \frac{39{,}530\ A}{2{,}000} \cdot \quad .372\ \Omega = 1{,}\ \ 62\ V$$

$$V_{ANSI} = C800 + (2 \quad \cdot \quad A \cdot \quad \Omega) = 1{,}300\ V$$

$$SLP2 = SLP1 = 10\%?$$

Remanence?

$$V_{SAT} = (K_{REM} \cdot K_{TD}) \cdot I_S \cdot (R_B + R_{CT})$$

$$V_{SAT} = (3 \cdot 1.8) \cdot \frac{39{,}530\ A}{2{,}000} \cdot \quad .372\ \Omega = \quad 73.3\ V$$

$$V_{ANSI} = C100 + (2 \quad \cdot \quad A \cdot \quad \Omega) = 600\ V$$

$$SLP2 = 90\%$$

## CT Size and Relay Setting

### Before → After

$$V_{SAT} = \left(1 + \frac{X}{R}\right) \cdot I_S \cdot (R_B + R_{CT})$$

$$V_{SAT} = 1 \quad \cdot \frac{39{,}530\ A}{2{,}000} \cdot \quad .372\ \Omega = 1,\ \ 62\ V$$

$$V_{ANSI} = C800 + (2 \quad \cdot \quad A \cdot \quad \Omega) = 1{,}300\ V$$

$$SLP2 = SLP1 = 10\%\ ?$$

Remanence?

$$V_{SAT} = (K_{REM} \cdot K_{TD}) \cdot I_S \cdot (R_B + R_{CT})$$

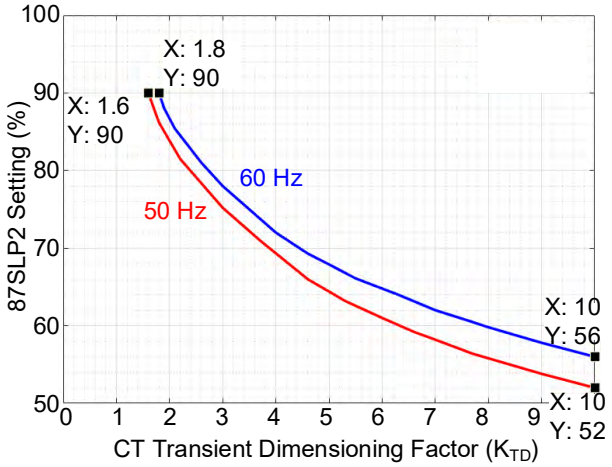
$$V_{SAT} = (3 \cdot 1.8) \cdot \frac{39{,}530\ A}{2{,}000} \cdot \quad .372\ \Omega = \quad 73.3\ V$$

$$V_{ANSI} = C400 + (2 \quad \cdot \quad A \cdot \quad \Omega) = 900\ V$$

$$SLP2 = 79\%$$

## Conclusion

- Both IEEE and IEC consider dc offset and remanence
- Use of CT models is neither ideal nor required
- Modern differential relay schemes can drastically reduce CT requirements
- Unambiguous application guidance results in precise
  - CT sizing
  - Relay settings


100
90
80
70
60
50
0
1
2
3
4
5
6
7
8
9
87SLP2 Setting (%)
CT Transient Dimensioning Factor ($K_{TD}$)
X: 1.8
Y: 90
X: 1.6
Y: 90
60 Hz
50 Hz
X: 10
Y: 56
X: 10
Y: 52

# Questions?