

Challenges One May Not Expect to Face When Applying Digital Relays

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I. Introduction

This paper presents few useful hints, which will help protection engineers and technicians to better understand, how perfectly normal work of the digital relay may sometimes bring unexpected results to the users in the field, during relay operation or during testing. It happens that some important details of the digital relays or important settings are misinterpreted, or overlooked, which may cause the confusion to the user with relay operation, or behavior. The user might even conclude and declare the digital relay response as a mis-operation, or a failure.

First, the paper explains why the CT and VT sizing remains important even in digital relay technology. Certain function of digital relay may be impacted with selected CT and VT taps, and may confuse the user with unexpected relay operation. While it looks that digital relay operating ranges are almost unlimited, stretching these operating ranges sometimes may cause unexpected relay performances, even unwanted effects.

Paper also examines some confusions, stemming from relay not meeting specification claims. Such claims arise sometimes, even during trivial testing of IOC, TOC, directional, underfrequency or distance functions. Cases are presented and explained, where relay seemed to “fail” without any obvious reason, when, it did not. Or relay didn’t meet specifications for unknown reasons, instead for overlooked reasons.

This paper is based on the practical experience of applying and testing digital relays and will give useful insights to engineers and technicians on ways to avoid unexpected operation, and better understand digital relay functionality, specifications and settings.

II. Measurement ranges of the digital relays

A. Maximum current and voltage ranges

This chapter focuses on what is happening in digital technology at extremes of the operating ranges. Specifically, at the signal high end, where signal gets chopped, or range above “signal clamping”. At the signal low end extreme, relay is “cutting off” the signal, since the processed signal is so weak that is in the range of a typical noise, i.e. digital device is not sensing signal at all. Proper CT sizing selection remains important in digital technology, as well, to ensure dependable protection.

Unlike electromechanical and solid-state (analog) protective relays, digital protective relays are used today not for protection purposes only, but also for metering, local and remote SCADA controls and monitoring, synchrophasors and other applications. Because of this, expectations are that relay will be able to measure very low signal (for accurate current and power metering) during system steady state conditions but will be able to deal with a high-level current during system fault as well. However, relays have measuring range and are accurate within this specified measuring range.

When we apply the certain digital relay, we usually do not pay attention at the measurement range of the current and voltage. We should. In the digital world, the measuring range is not infinite: the range between minimum and maximum relay values is determined and values outside this range may impact relay operation. Typically, measuring range for currents, depending on the relay model will be:

Transient performance of CTs including DC offset in fault currents is reflected in IEC 61869-2:2012 (replaced IEC 60044-6) “Instrument transformers – Part 2: Additional requirements for current transformers” and in [1] IEEE C37.110-2007 “Guide for the Application of Current Transformers Used for Protective Relaying Purposes”. These documents specify conditions to avoid CT saturation and estimate CT time-to-saturate to ensure application is secure.

Figure 1 above depicts a dilemma for the P&C engineer to select CT ratio:

- With a regular practice based on the selecting CT ratio, such as, at maximum load current CT will deliver nominal secondary current may cause problems, where fault current is much higher $20 \times I_n$. First of all, CT will experience additional errors and secondly there is a possibility of the CT saturation.
- In some utilities it is a normal practice to select CT ratio much higher than the maximum load current, especially for transformer differential application. This practice helps to avoid CT saturation, but is creating other problems, such as loss of protection sensitivity during low current faults (for example high-resistive faults) and loss of metering sensitivity.
- On the other side, in some utilities more focus is on getting metering data as sensitive as possible to provide operators with analog values. Digital relays are designed today to withstand continuous current $3-4 \times I_n$, therefore there is no danger to employ such practice, if maximum fault current is less than $20 \times I_n$ and within measuring range of the relay.

Figure 2 below depicts a case, where relay maximum analog-to-digital (A/D) conversion value is $30 \times I_n$. In blue color are shown waveform and phasor magnitude of the true CT secondary current, where in red are shown waveform and phasor magnitude after clipping. As $30 \times I_n$ is expressed in RMS terms, it means that samples above $30 \times I_n \times \sqrt{2} = 42.426 \times I_n$ are clipped and held at this value. Even steady state fault current is at $30 \times I_n$ not exceeding conversion range, due to DC offset in fault current, first 10 cycles we can see significant reduction in the phasor magnitude of the clipped current. In the first cycle of the fault clipped current phasor magnitude is reduced to $16.37 / 30.12 \times 100\% = 54\%$ of the true magnitude of the fault current.

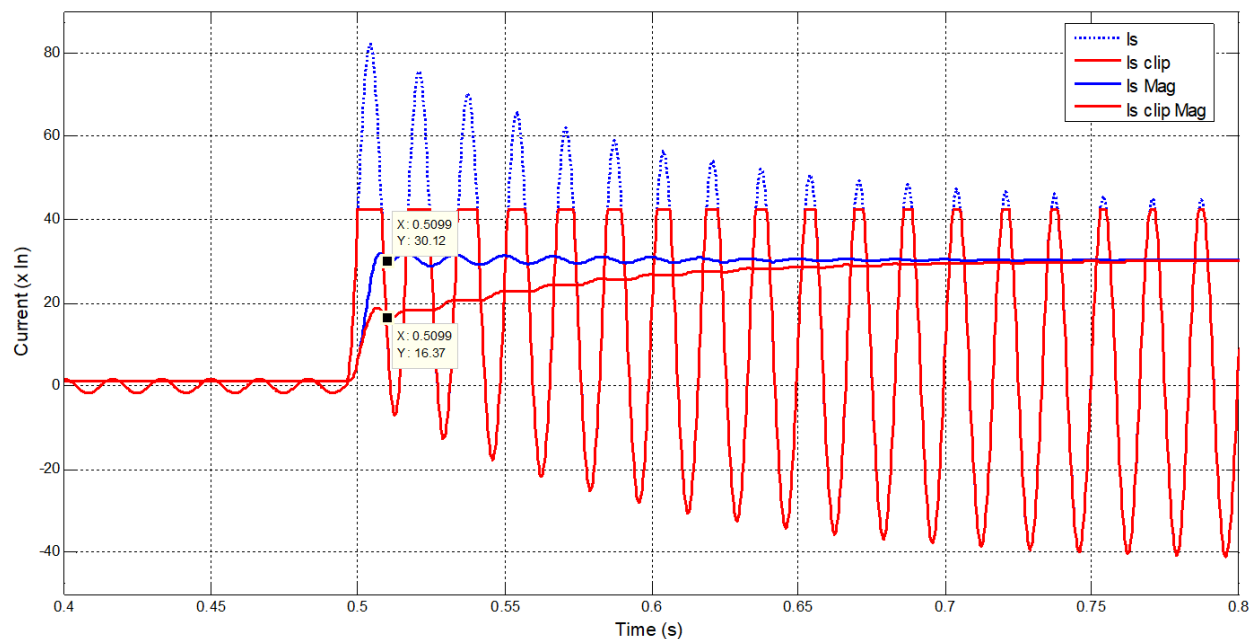


Figure 2. Clipping effect when current exceeds conversion range

It's not hard to foresee consequences of such clipping:

- Possibility of miscoordination with downstream OC relays
- Possibility of bus differential misoperation during external fault, where faulted feeder current may exceed conversion range but other feeders, contributing to the fault current may not exceed conversion range.
- Possibility of directional OC misoperation, because phasors angles are affected same as phasors magnitude.
- Generation of harmonics as a result of clipping, which can affect functions using harmonics, such as 2nd harmonic inhibit in transformer differential.

B. Minimum current and voltage ranges

A less considered and less analyzed phenomenon of “Low Level” current and voltage ranges often can surprise digital relay users.

“IEEE Standard Requirements for Instrument Transformers” [8] indicates accuracy requirements for relaying class CTs only at rated current (3% error for C and T class CTs) and at 20 times rated current (10% error for C and T class CTs) only. It is silent for accuracy for lower than rated currents and this is what we are not paying attention to. However, performance at lower than rated current is important for sensitive protection, what we are trying to achieve with digital relays technology. But we can get some idea of CT performance at lower currents from metering class CT requirements which are defined much better.

Figure 3 shows the accuracy limits for a metering class CT with rating factor of 4.0. The limit of permissible error in a current transformer accuracy class has one value at 100% rated current and allows twice that amount of error between 10% and 100% rated current [3]. But even for metering class CTs error for current less than 10% rated current is not defined at all. Typically, this is the area from the extreme left (zero current value) to the cutoff value of the current as specified in relay. Below its cutoff value, relay ignores the data samples and use null values for computing the current phasors.

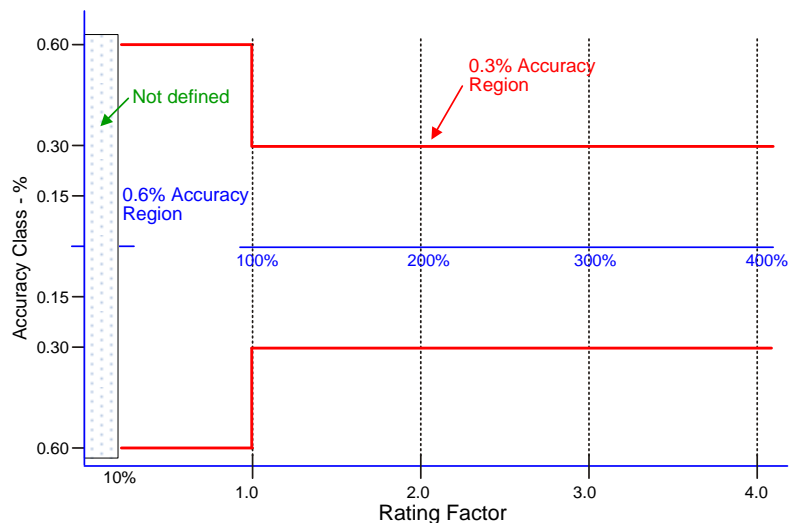


Figure 3. CT accuracy at different levels, including the not-defined region at low level

While CTs experience inaccuracy at higher magnitudes of currents due to saturation, specifically significant magnitude and phase errors are present, CTs exhibit substantial angular errors at lower

currents. A sample CT profile of magnitude errors at high currents is illustrated in the Figure 4a. Illustration of sample CT phase angle errors at low current is shown in the Figure 4b.

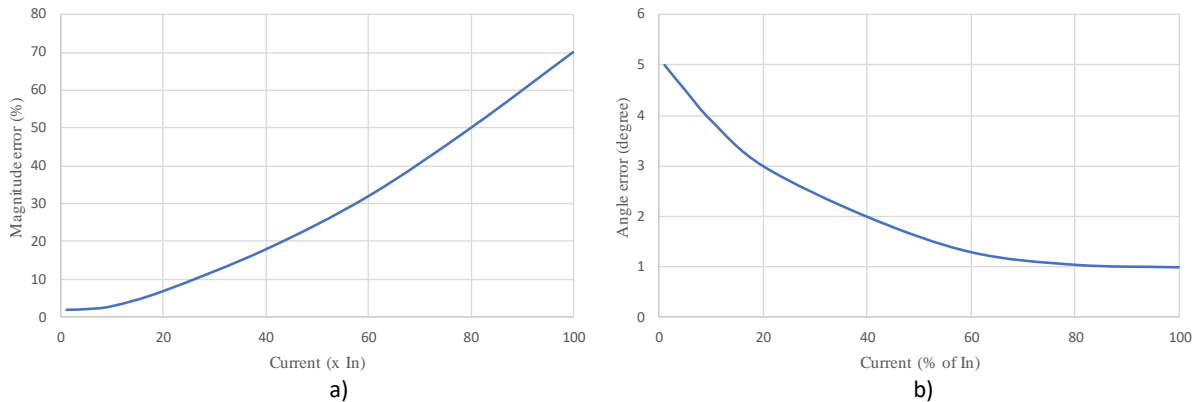


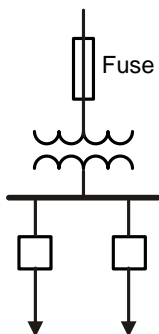
Figure 4. CT magnitude (a) and phase (b) errors at different current level: sample profile

While magnitude errors can result in relay failure to operate due to CT saturation at higher currents, due to relay reading lower current magnitudes than real magnitude, angular error can compromise directionality in relays, and can compromise all other protection elements depending on voltage signal.

C. Impact of minimum range cutoff on relay functionality

Figure 5 illustrates the impact on relay operation for low end currents, particularly nearby or below current cutoff level. Transformer is fused on its high voltage side and is protected against “transformer single phasing”. Each of the F1 and F2 relays should trip on “negative voltage unbalance” independently (voltage unbalance – as IEEE function 47 initiated by power transformer blown fuse). To the user surprise, a relay may “see” a sudden change of voltage, but without any change in current, and can wrongly conclude that this is a Loss of Potential. Because of this, relay would block tripping on all voltage related protection elements, like tripping on function 47, but also would block any distance protection and directional protection. This could result in declaring relay misoperation.

In this particular case, a blown fuse on the transformer high-side resulted with one feeder (F1) tripping, while the other feeder (F2) did not. Major factor was a load current, being on one feeder (F1) above the current cutoff (or with a current resolution sensitive enough to recognize the current change), whereas on the other feeder (F2) the load current was below the current cutoff (or with a current resolution below sensitivity to recognize the current change): consequently, relay declared that this is a Loss of Potential condition.



Parameter	Feeder 1	Feeder 2
Load	> cutoff	<cutoff
Voltage change on blown fuse	Detected	Detected
Current change on blown fuse	Detected	Not detected
Loss of potential (LOP)	Not operated	Operated
Feeder fault	Trip	No trip

Figure 5. Impact of low load current on the relay functionality

Due to large CTs, which are addressing CT saturation issues, low load currents may be hardly measurable by the relays - protection tripping during transformer single-phasing can be unexpectedly compromised. Directional elements and distance protection can also be similarly blocked, if we had large CTs in the protected line during the fault on adjacent line.

III. Understanding specifications and functionality

A. Hysteresis

Hysteresis is applied in digital relays for voltage and current based elements to prevent element chattering when operate signal is close and fluctuating near pickup level of the element. While in E/M and static relays this was inherited by electromagnetics and operational amplifiers characteristics, in digital relay this is somewhat artificial. This “artificial” characteristic is needed due to high accuracy and high resolution of the analog-to-digital conversion.

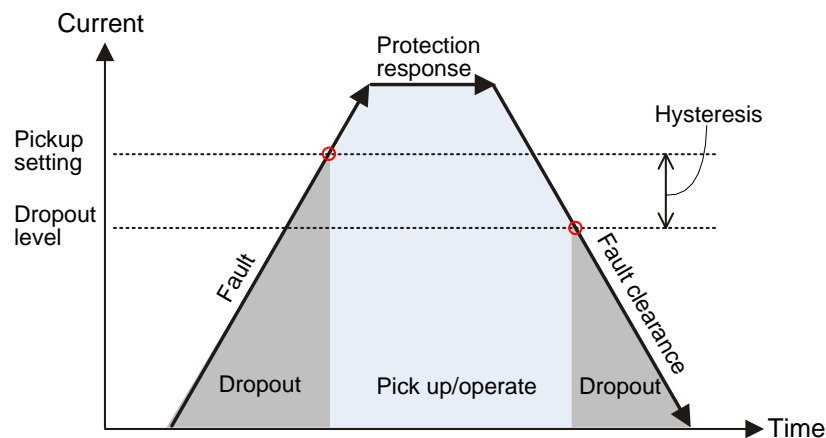


Figure 6. Hysteresis applied to overcurrent elements illustration

As shown in the Figure 6 above, below the pickup level of the element there is another level defined by the hysteresis margin. To operate the element, operating quantity must exceed the pickup setting, but for dropout operating quantity has to be below this dropout level. Typically, hysteresis is 2-3% and is defined in product specifications but in some products or elements it can be settable. Hysteresis can create some confusion, especially during testing.

Figure 7 below illustrates how hysteresis can cause confusion during OC element accuracy testing. Using conventional test set, we can see that 5A sinewaves inception looks different in different phases. While phase A starts at zero-crossing appearing as perfect sinusoid, phases B and C are instantly and artificially “jumped” to some point and after this point B and C phases continue smooth sinusoid. Depending on the digital relay filtering and phasor estimation, this artificial jump can create transient error, affecting test outcome. We can see that phase B current magnitude overshoots to 5.272A, which is 5.4%. This is well above typical digital relay current accuracy of 0.5-1.5%.

If someone attempts to test OC element accuracy with a such step change in currents say 3% above the pickup setting, expecting OC element not to operate - relay will “fail” because current overshooting will pickup the element but will not allow to dropout because current magnitude will never drop below hysteresis level. In general, step change in currents and voltages is not an appropriate method to test accuracy of instantaneous elements, because of sinewave inception transients. Current or voltage ramp up or ramp down are more appropriate here.

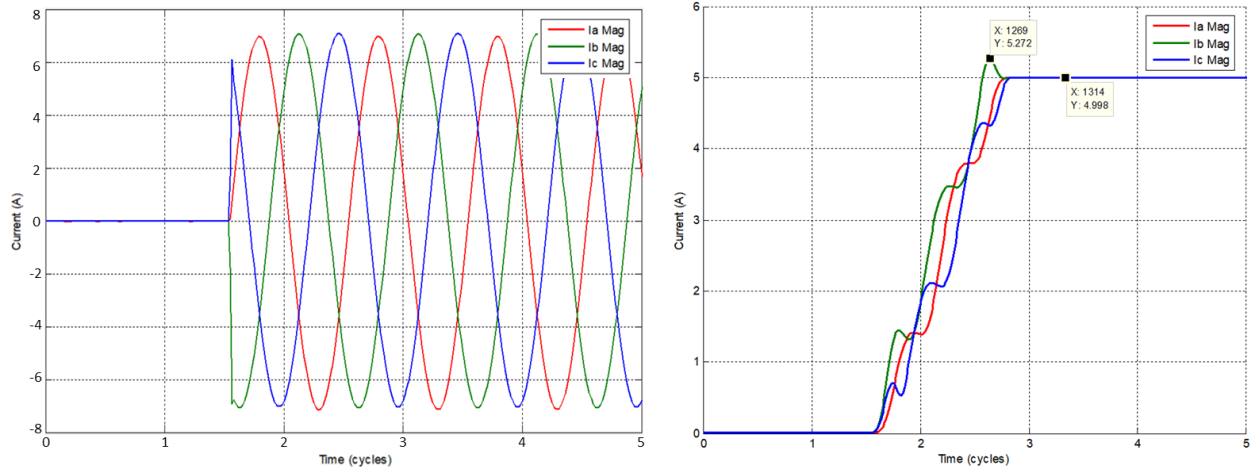


Figure 7. Currents step change with conventional test set to test OC pickup

B. Accuracy improvements

Table 2 below gives typical errors for time overcurrent relays excluding CT measurement errors, system transient errors and test simulation errors.

Error type	Relay technology		
	E/M	Static	Digital
Magnitude overshoot	10%	5%	2%
Overshoot time	0.05s	0.03s	0.02s
Pickup error	5%	3%	1%
Timing error	7-15%	5-7%	3-4%
Coordination safety margin	0.1s	0.05s	0.03s
Typical coordination time	0.4s	0.3s	0.2s

Table 2. Typical errors in time overcurrent relay

We can notice that digital relays offered us a significant improvement in the performance compared with previous generations, which allowed us faster, more accurate and more secure protection. This is achieved by better hardware, better filtering and better algorithms. It also gives user better description of the functionality, giving much more details on the functionality with detailed logic diagrams, specifications and applications advises. However, it requires user to understand functionality of the specific product in order to avoid any mis-interpretations and confusions.

C. Timing

Nothing can be easier than TOC timing testing...but why digital relay sometimes “fails” timing test? Typical stated curve timing accuracy in digital relays is “3-4% or 0.5-1 cycle, whichever is greater”. Important thing here is term “curve timing accuracy”, meaning how accurate relay will calculate time to time out and issue a trip command. The common misconception here is what to consider the test starting time – is it fault injection or anything else? Yes, it’s anything else – it starts from the element start (pickup) flag, not from the start of injection.

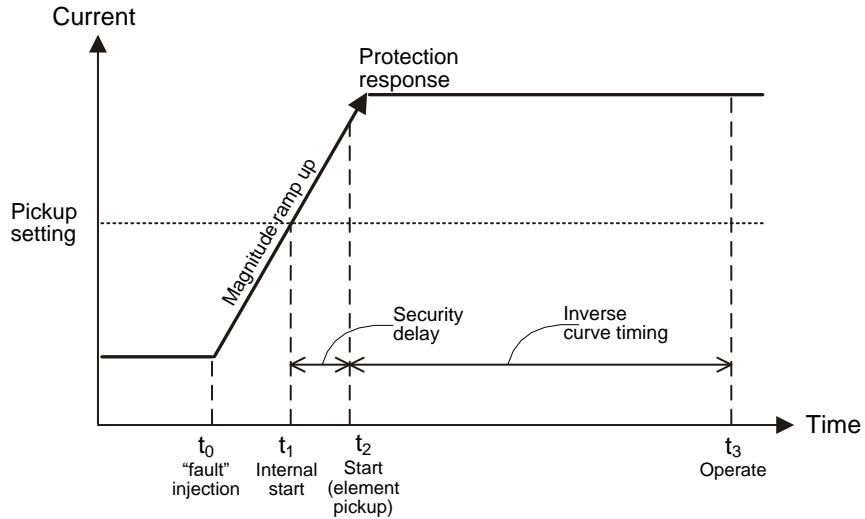


Figure 8. TOC timing

Figure 8 illustrates steps in digital relay to assert Start and Operate flags. At time t_0 currents are increased from pre-fault to fault. Current phasor magnitude starts increasing and at time t_1 magnitude becomes above TOC pickup setting. How fast magnitude will transverse from t_0 to t_1 depends on the specific relay filtering and phasor estimation algorithm. Generally, for digital relay it takes 1 to 1 ½ cycles to reach new magnitude level after step change in currents.

However, the pickup flag is not asserted at time t_1 because there is a security delay, needed to prevent erroneous activation due to transients. This security delay is needed again due to much faster response in digital relays, compared with previous generations. Security delay typically is ¼ to ½ cycle. Finally, at time t_2 pickup flag is asserted, and this is where timer starts counting. Between t_2 and t_3 is what really claimed in digital relay as “timing accuracy” for inverse time overcurrent characteristics, not time between t_0 and t_3 .

Here is real life testing example where digital relay “failed” the inverse time overcurrent timing accuracy specifications. Technician was testing Neutral TOC set with IAC very inverse curve, which is defined by equation:

$$t = TDM \cdot \left[A + \frac{B}{(I/I_{pkp}) - C} + \frac{D}{((I/I_{pkp}) - C)^2} + \frac{E}{((I/I_{pkp}) - C)^3} \right] \quad \text{Equation 1}$$

For IAC very inverse curve, $A=0.09$, $B=0.7955$, $C=0.1$, $D= -1.2885$ and $E=7.9586$. With a user setting of $TDM=0.77$, $I_{pkp}=500A$ and injection $I=1000A$, expected operate time would be $t=1010ms$. However, technician reported relay operated in 1065ms, yielding timing error of:

$$E = \frac{1065ms - 1010ms}{1010} \cdot 100\% = 5.44\%, \text{ exceeding digital relay timing accuracy claim of } 3.5\%.$$

Did relay fail? Let’s dig in to analyze.

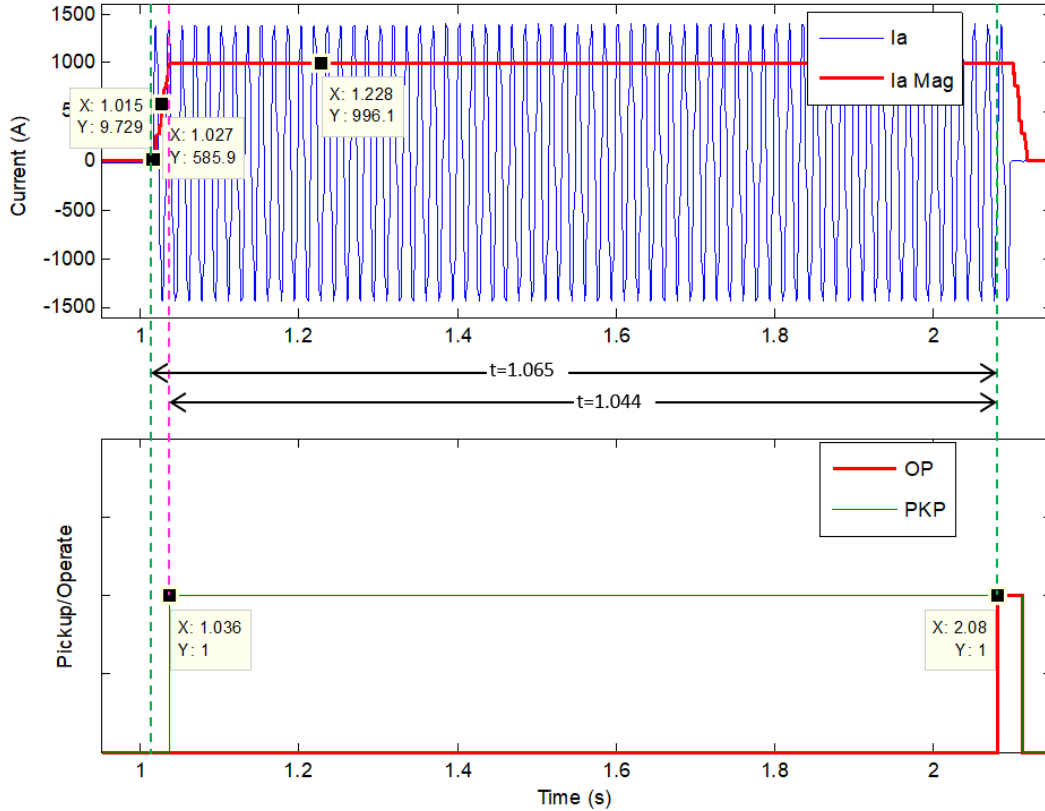


Figure 9. Analysis of TOC timing "Failure"

First of all, we can notice from Figure 9 that from the moment $t_0 = 1.015s$ till current magnitude became above pickup $t_1 = 1.027s$ it elapsed 12ms. Another 9ms was needed for security delay, resulting in Pickup flag asserting in 21ms since current inception. Therefore, inverse characteristic timing becomes 1.044ms instead of 1.065ms if we count timer starting from Pickup flag. Another contributing factor is that relay measured 996A primary, instead of expected 1000A. Possibly this is due calibration of the test set or relay itself but expected operate time with 996A is changing now from 1010ms to 1021ms. Therefore, realistic digital relay error is:

$$E = \frac{1044ms - 1021ms}{1021} \cdot 100\% = 2.25\%, \text{ within digital relay timing accuracy claim of } 3.5\%.$$

D. Importance of proper testing methods and analysis

Many elements use sequence-components, which may affect function under the test. Sometimes P&C engineers don't realize this, which causes unexpected results. One example we want to illustrate is related to the testing of the distance function. We all know that classic MHO function is comparing following quantities for phase distance AB loop as an example:

$$(I_A - I_B) \times Z - (V_A - V_B) \text{ and } (V_A - V_B)_M \quad \text{Equation 2}$$

where $(V_A - V_B)_M$ stands for the memory voltage.

Looking at this equation, one can think we should care about phases A and B voltages and currents only, when doing testing. This, however, is not a case. Although, there are few options for polarize distance elements, most commonly used is positive-sequence voltage calculated, from all 3 phases to polarize all 6 loops of the phase and ground distance function. This is done for several reasons: a) positive-sequence voltage is remaining stable during fault and not affected by fault transients compared with self-polarized;

b) it provides dynamic expansion of the characteristics. Even when positive-sequence memory voltage expires, relay becomes self-polarized but still positive-sequence self-polarized. What it means is that relay calculates positive sequence voltage V_1 and then shifts it by appropriate angle to obtain V_{1A} , V_{1B} , V_{1C} , V_{1AB} , V_{1BC} and V_{1CA} for all 6 loops. What it also means is that relay is sensitive, if positive-sequence voltage angle is shifted dramatically by arbitrarily shifting faulted or healthy voltages from pre-fault to fault.

Especially challenging may be testing of the relay response with fault resistance to estimate fault resistive coverage due to MHO/QUAD expansion of the particular relay for a particular application. Interesting to note is that resistive coverage depends not only on the relay reach but also on the system impedance behind. Preferred way to estimate fault resistive coverage for a specific application is to simulate resistive fault using appropriate simulation tools such as RTDS, PSCAD, ATP and other to play back to the relay. Other short circuit programs may give fault static phasors, allowing to inject these phasors using test sets. The question is how to evaluate relay either response is correct or not during MHO/QUAD expansion, when dynamic characteristic is not plotted by any tool?

Here is an example how to estimate relay response. During AB fault with a fault resistance of 1.2Ω at 20% of the $3\Omega \angle 85^\circ$ transmission line, phase distance zone 1 with a $2.55\Omega \angle 85^\circ$ reach didn't operate at all. Phase distance zone 2 MHO with a $4\Omega \angle 85^\circ$ reach setting picked up initially, but dropped out after memory voltage expired, resulting in NO zone 2 operation. Table 3 below gives fault phasors recorded by the relay in secondary values.

	Pre-fault	Fault
Va	$66.4V \angle 0^\circ$	$55.7V \angle -38^\circ$
Vb	$66.4V \angle -120^\circ$	$25.5V \angle -115^\circ$
Vc	$66.4V \angle 120^\circ$	$66.4V \angle 120^\circ$
V1a	$66.4V \angle 0^\circ$	$46.5V \angle -13^\circ$
Ia	$0A \angle 0^\circ$	$6.84A \angle -28^\circ$
Ib	$0A \angle 0^\circ$	$6.84A \angle 152^\circ$
Ic	$0A \angle 0^\circ$	$0A \angle 0^\circ$
I1a	$0A \angle 0^\circ$	$3.95A \angle -58^\circ$

Table 3. AB fault with 1.2 ohms fault resistance phasors

It's was explained in many publications before [3] that phase distance expansion depends on the positive-sequence impedance of the source behind the relay for relays which are polarized with positive-sequence voltage. Expansion, or dynamic characteristics is different for a different type of the fault. For a phase-to-phase faults initially MHO expands to full Z_{1s} impedance and reduces expansion to $Z_{1s}/2$ after memory expires per [5]. However, source impedance may be unknown during testing or real relay operation— how one can validate relay response?

Source Z_{1s} can be estimated using following equation:

$$Z_{1s} = -\Delta V_1 / \Delta I_1 \quad \text{Equation 3}$$

Where ΔV_1 is the change in the positive-sequence voltage from pre-fault to fault and ΔI_1 is the change in the positive-sequence current. Using fault values from the Table 3, we can calculate source positive-sequence impedance $Z_{1s} = - (66.4V \angle 0^\circ - 46.5V \angle -13^\circ) / (0A \angle 0^\circ - 3.95A \angle -58^\circ) = 6.02\Omega \angle 85^\circ$. Now we know how MHO characteristic expands at the beginning of the fault and after memory expires. Figure 10 below demonstrates the expansion of the MHO during this fault - we can explain why phase distance picked up initially but dropped out when memory voltage expired. The locus is inside full pre-fault memory voltage

dynamic characteristic (green line) but is outside the characteristic after memory voltage expired (blue)

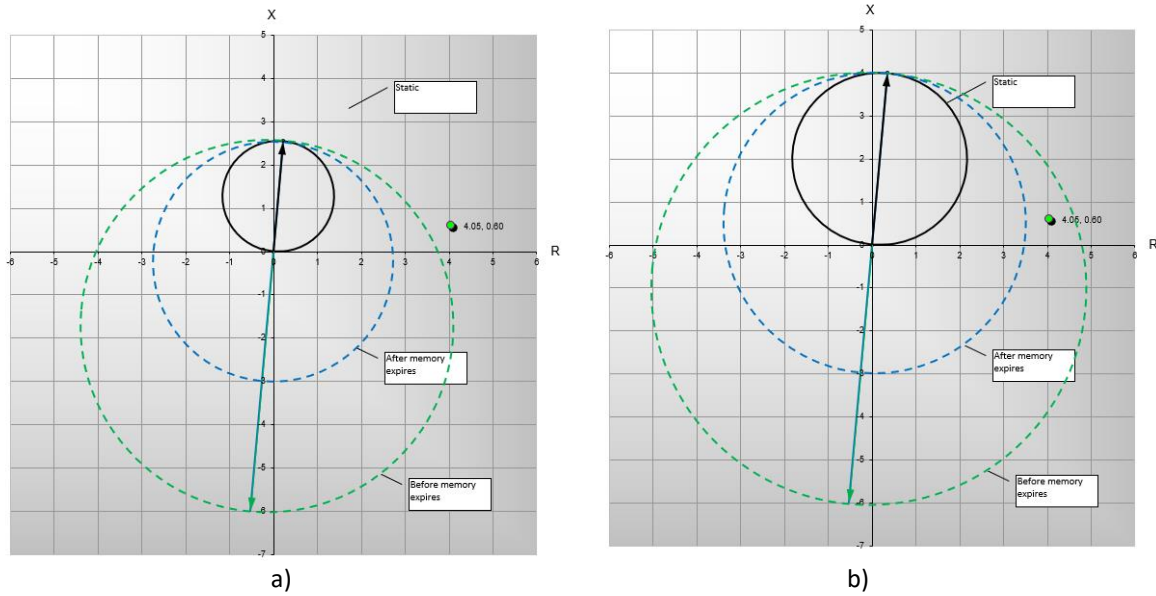


Figure 10. Phase distance zone 1 (a) and zone 2 (b) MHO expansion for AB fault with 8Ω fault resistance

Actually, phase distance dynamic characteristic during fault depends on 2 factors: zone reach to source Z_{1s} impedance and fault type. Z_{1s} will dictate how far MHO expands into 3rd quadrant and inherently into 1st and 2nd quadrant, using memory voltage but fault type dictates the characteristic after memory voltage expires. As noted above, during phase-to-phase faults phase distance remains expanded even using actual positive-sequence voltage. Phase distance MHO will return to the “static” characteristics during 3-phase faults only, because fault loop voltage V_{AB} will be equal to V_{1AB} voltage.

Knowing phase distance zone expansion, we can now plot expanded characteristics to visualize if apparent impedance is within expanded zone or not, as it's shown in the Figure 10 above. Alternatively, we can estimate if impedance locus is within the zone or not. First, we can estimate faulted loop apparent impedance by simply dividing V_{AB} phasor by I_{AB} phasor for the AB fault. In our test case it will yield $Z_{AB} = (55.83V \angle -11.6^\circ) / (13.68A \angle -28.2^\circ) = 4.08\Omega \angle 16.6^\circ = 3.91 + j1.17 (\Omega)$.

Secondly, we can now estimate if apparent impedance is within the expanded MHO characteristics using classic circle equation:

$$(x - a)^2 + (y - b)^2 = r^2 \quad \text{Equation 4}$$

Where x and y are coordinates of any points completing the circle with a radius r , while a and b are coordinates of the circle center. If we use our apparent impedance coordinates calculated above as x and y with a known circle offset, sum of squares less than r^2 would mean apparent impedance is inside expanded characteristics. When sum of squares is greater than r^2 , it means apparent impedance is outside expanded characteristics. Using zone 2 values as an example, we can prove it.

Before memory expires:

- $r = \frac{(Z_R + Z_{1s})}{2} = \frac{(4 \angle 85^\circ + 6 \angle 85^\circ)}{2} = 5 \angle 85^\circ$
- MHO circle offset is: $Z_R - r = 4 \angle 85^\circ - 5 \angle 85^\circ = 1 \angle 265^\circ = -0.087 - j0.996$ which are a and b values of Equation 4 above.
- $(3.91 - (-0.087))^2 + (1.17 - (-0.996))^2 = 20.67 < r^2 = 25$ inside the characteristics

After memory expires:

- $r = \frac{(Z_R + Z_{1S})}{2} = \frac{(4 \angle 85^\circ + 3 \angle 85^\circ)}{2} = 3.55 \angle 85^\circ$;
- MHO circle offset is: $Z_R - r = 4 \angle 85^\circ - 3.5 \angle 85^\circ = 0.5 \angle 85^\circ = 0.044 + j0.498$ which are a and b values.
- $(3.91 - 0.044)^2 + (1.17 - 0.498)^2 = 15.4 > r^2 = 12.25$ outside the characteristics

Same approach can be applied to a ground distance function as well. Equation 3 can be used to calculate source zero-sequence impedance, similar to the positive-sequence impedance.

IV. Understanding specific product behavior

A. RMS or fundamental frequency phasor?

P&C engineers still today are thinking RMS measurements, because this is what was in E/M and static relays. But digital relays work on phasors, where some functions have a choice of RMS or phasor. Why and where we need to pay attention?

As mentioned above, digital relays are very accurate, much more accurate compared with a predecessor. Better accuracy of the protective functions is achieved by extensive filtering to remove noise and system transients, harmonics, calibration, tracking to the system frequency and finally by calculating fundamental frequency phasors. Therefore, digital relays can estimate currents and voltages much more accurate, which is improving accuracy of the fault location, differential measurements, overcurrent, undervoltage and many other functions.

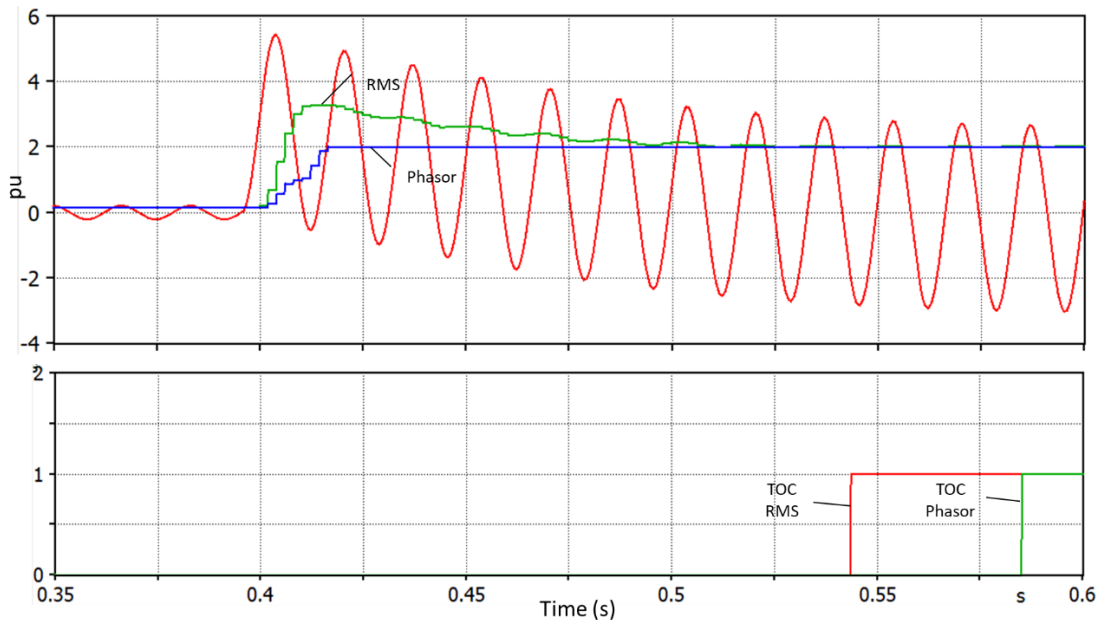


Figure 11. Fundamental phasor and RMS illustration

On the contrary, RMS measurements should include harmonics, DC offset and other transients to give an estimation of the impact of the power system on the protected equipment, for example thermal heating. In spite of majority of protective functions in the digital relays use fundamental frequency phasor, some function require RMS values as well. E/M and static relays were always using RMS values, therefore digital relays offer this option as well. When coordination overcurrent element with a downstream relay, it's always a good idea to check if this relay is a digital relay or E/M or static relay. In case this is E/M or

static relay, it's good to use RMS values as an input to OC elements. If this is a digital relay, fundamental frequency phasor is a better choice.

Figure 11 above is highlighting the difference in fundamental frequency phasor and RMS measurements and impact on the TOC function using same inverse time characteristics timing curves, when current has significant DC offset. We can see that RMS measurement is significantly overshooting at the beginning, making TOC operating on the RMS value operating 42ms faster than TOC operating on phasor values. This may create coordination problems, if overlooked. We can also notice how well modern relays are removing DC offset, making fundamental frequency phasor very precise and steady.

B. Frequency elements testing

Testing of underfrequency, overfrequency and rate-of-change-of-frequency requires some caution to avoid erroneous results. Most of protection elements are designed to detect change from normal condition to a fault condition, current, voltage, impedance, which occur instantly. Frequency elements are responding to the system frequency change, which cannot change very rapidly in the conventional power system due to system inertia. Frequency measurement may be affected by the system transients (faults, switching), noise, measurement errors – erroneous frequency measurement may cause large power outages due to nuisance operation of the frequency elements.

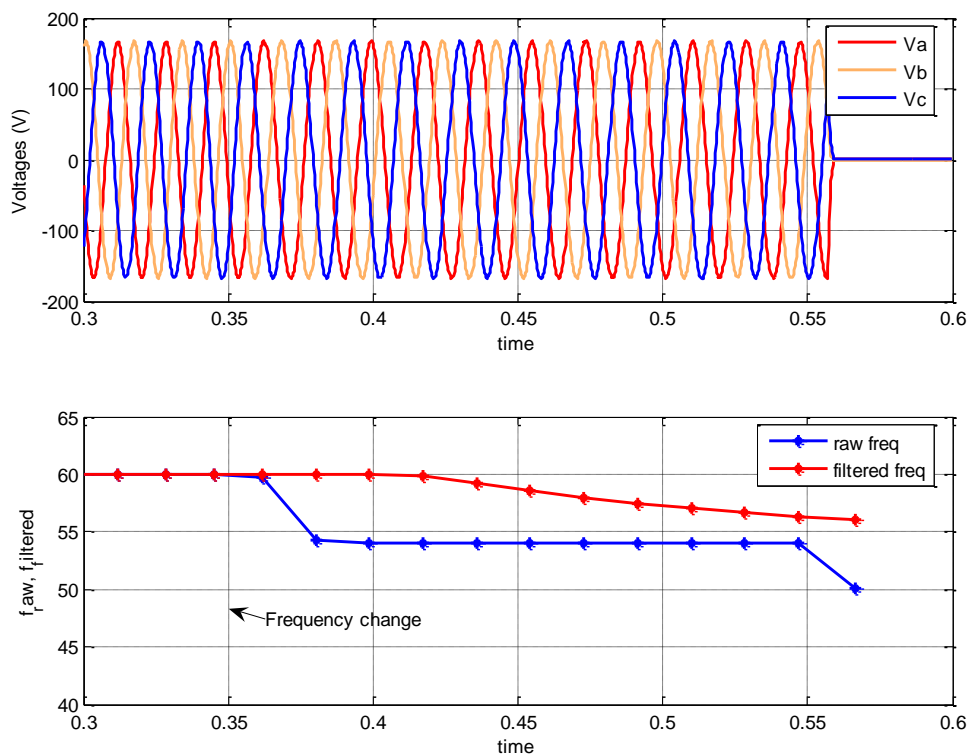


Figure 12. Underfrequency test

Therefore, digital relays apply sanity check to validate frequency measurement and prevent nuisance operation of the frequency elements. This should not be overlooked during routine testing of the frequency elements. Here is an example of the typical mistake during testing: technician was testing underfrequency element with a 57Hz pickup setting and 200ms delay. He applied a step change in the voltage and current signals from 60Hz to 54Hz – relay “failed” testing because didn’t operate in 200ms

delay + relay stated pickup timing. Figure 12 below demonstrates voltage waveforms where at 0.35s frequency was changed in one step from 60Hz to 54Hz and also frequency measurements.

We can see that raw frequency calculated by the relay from the voltage zero-crossing changed from 60Hz to 54Hz in less than 2 cycles, however relay frequency took another 50ms to start slowly adjusting frequency value, which delayed operation of the UF. Is it a “fail” test and why did it take so long?

It appears that this relay is first validating measured frequency and secondly is post-filtering measured value. For example it’s checking that df/dt is not exceeding 20Hz/s to ensure wrong measurement is not leaking into frequency value used by UF function. Preferred method of the frequency elements testing is a frequency ramp, not a step change.

V. Conclusions

Digital relays offer much better accuracy and timing characteristics, compared with E/M and static relays. They also provide much better visibility into what signal relay is responding to, what relay is measuring and all sequential digital indications about elements operation from pre-fault to post-fault. However, sometimes technical characteristics and functionality of digital relays are not understood correctly, especially when it comes to testing of the digital relay.

Attention must be paid to the specific relay technical specifications and method of testing of the specific element. It was shown above that some test methods are causing digital relays ‘failures’, where it’s not really a case.

VI. References

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8. IEEE Std C57.13™-2016 “IEEE Standard Requirements for Instrument Transformers”

VII. Biographies

Miroslav Ristic has been with System Protection of Pacific Gas and Electric Company for more than fifteen years. Currently, he is the technical lead in Distribution System Protection with emphasis on San Francisco-East Bay area, supporting numerous venues of utility business, namely: Distribution Switching Centers and Distribution Operations Department on clearances and event analysis, Distribution Planning Department on relevant protection issues, Design, Substation Engineering and Construction Departments on protection aspects of the new and ongoing projects. He has been awarded by PG&E for innovation and contribution in design standards, special protection schemes, and unique scheme for audio noise reduction in transformers. Prior to this, he was an Application

Consultant with GE Multilin in Toronto, Canada, where he provided field support and protection expertise to the utilities and industrial companies worldwide. He gained his practical experience working in protection on the Electric Power System of Yugoslavia. He has received a master's in electrical and computer engineering degree from University of Novi Sad, Yugoslavia, and has more than 35 years of experience in relay protection. He is a Registered Professional Engineer in California, and recently put on hold his P.Eng. license in Ontario, Canada.

Harjeet S. Gill received his B.Sc. and B.E. Honors (Electrical Engineering) degrees from Panjab University, India, M.Sc. and Ph.D. degrees from University of Saskatchewan, Canada, M.B.A. degree from Cameron University, USA, and Certification in Project Management from University of the Pacific, Stockton, USA. He has comprehensive professional experience of working in research, industry and academics. This includes association as teaching and research assistant in university, Applications Engineer at ABB Inc. in Santa Clara, CA and Allentown, PA, and as Protection Engineer at Pennsylvania Power Light Utility, Allentown, PA before his present assignment as Senior Protection Engineer at PG&E. He has been associated in diverse areas of power systems including load-flow and stability studies for system interconnections, energy management systems, defining and implementing relay algorithms and their testing within relay manufacturing environment, field tests for high-impedance fault detection, process development and support systems (version control and testing software), and reviewing/updating/implementing utility protection practices and principles. Technical publications contributed by him have been recognized with Best IEEE Paper and IEE's premium paper awards. In current position, he is engaged in distribution system protection and provides support to diverse engineering groups - distributed generation, operations and planning. He is a registered Professional Engineer in California and a licensed Project Management Professional with PMI.

Iliia Voloh received his Electrical Engineering degree from Ivanovo State Power University, Russia. He is currently an applications engineering manager with GE Grid Solutions in Markham Ontario, and he has been heavily involved in the development of UR-series and 8-series of relays. His areas of interest are current differential relaying, distance relaying, advanced algorithm and advanced communications for protective relaying. Iliia authored and co-authored more than 40 papers presented at major North America Protective Relaying conferences. He is a recipient of the best paper award at Georgia Institute and Technology Protective Relaying Conference in 2012. Iliia is a senior member of the IEEE, member of the IEEE PSRC main committee, a member of the IEC TC 95 committee and a member of the CIGRE B5.65 working group.