

Fault Coverage of Memory Polarized Mho Elements with Time Delays

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Abstract

This paper analyzes the effect of time delays on the fault resistance coverage of memory polarized distance elements. A high voltage, electrically short, transmission line with a permissive overreaching transfer trip (POTT) protection scheme and mho step distance backup will be analyzed to show the reduction in fault resistance coverage caused by capacitive voltage transformer blocking logic, communications delays, and time delays associated with step distance backup. The reduction in fault coverage due to memory voltage decay will be compared to the approximate arc fault resistance encountered for faults on the transmission line. Solutions to deficiencies in the fault resistance coverage will be examined such as replacing the POTT scheme with DCB or quadrilateral distance elements to create a more dependable protection scheme.

Introduction

Implementing a communications assisted tripping scheme with modern relays requires the selection of multiple time delays that impact fault resistance coverage. Time delays result from relay pickup time, communications delays, or timers applied by a relay-setting engineer to increase either dependability or security. Increasing the time delays associated with the communications scheme can have a significant impact on the fault resistance coverage.

Initial performance of a POTT communications scheme will be studied with a system shown below in Figure 1. The scheme is implemented according to the standard settings and logic used by the client. Standard settings include a zone 2 set at 100% + 50% of the protected transmission line and a reverse zone 3 set at 200% of the remote end overreach. These standard settings lead to a zone 2 reach of $0.53\Omega_{sec}$ and a zone 3 reach of $0.7\Omega_{sec}$. Additionally, the POTT scheme for this line is required to trip within 10 cycles due to system stability requirements.

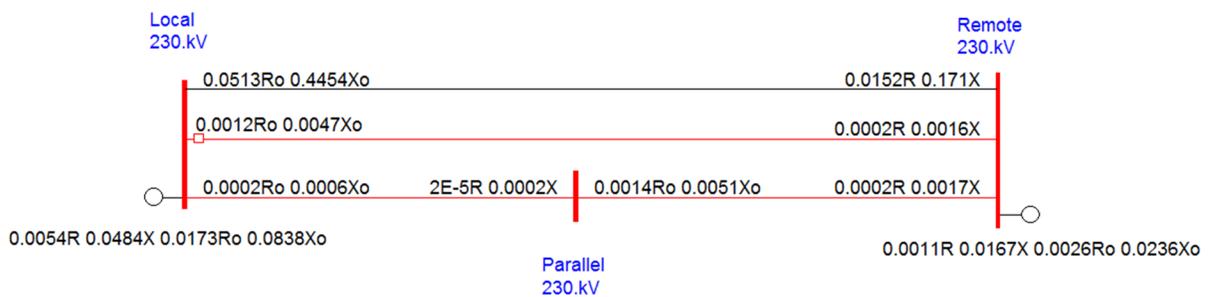


Figure 1 System One Line

The protection scheme for this line needs to securely and dependably trip for all faults on the transmission line with high speed and restrain tripping for the short line located at the remote bus. With the system described in Figure 1, relay performance when only considering the steady state solution will fail to clear remote bus fault conditions before the critical clearing time when a

standard 150% zone 2 reach is used. This particular fault case is plotted below in Figure 2. The same system will be found to clear these faults when the memory voltage polarization is included in the relay simulation.

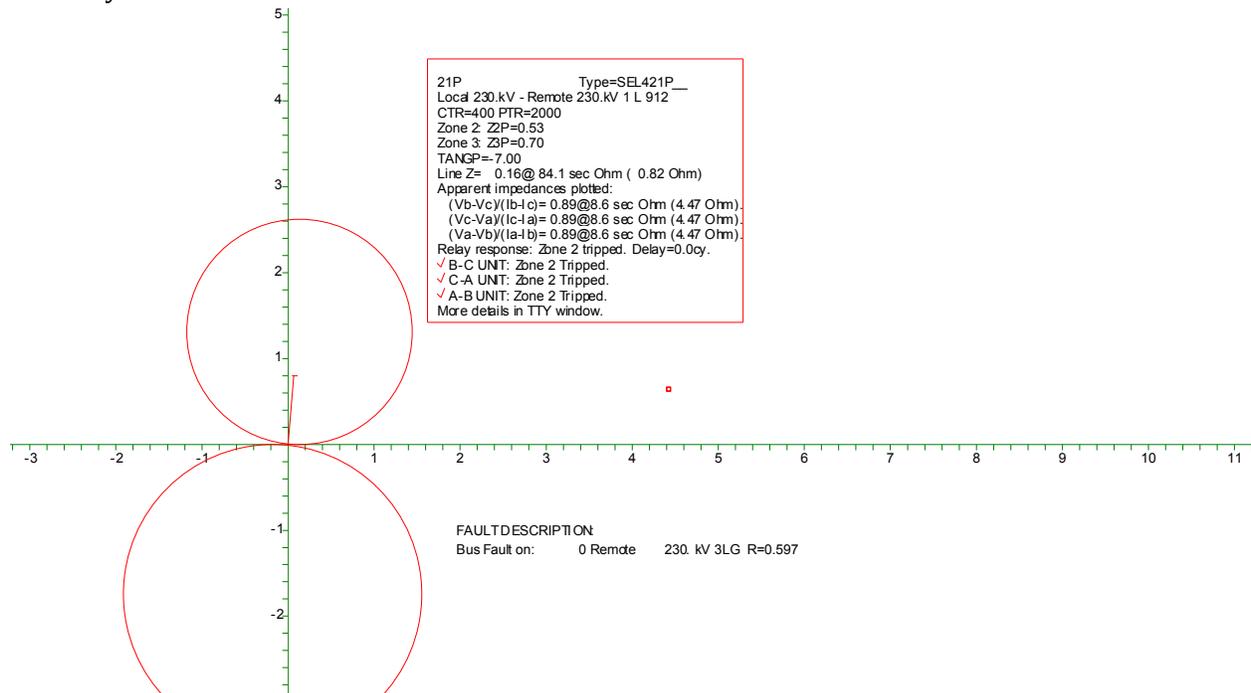


Figure 2 Remote Bus Fault

Calculating Fault Resistance Coverage

Performance of the communications assisted relay scheme requires the following function blocks to simulate a fault with memory voltage elements. For simplicity, this simulation neglects the impact of transient effects on the steady state solution.

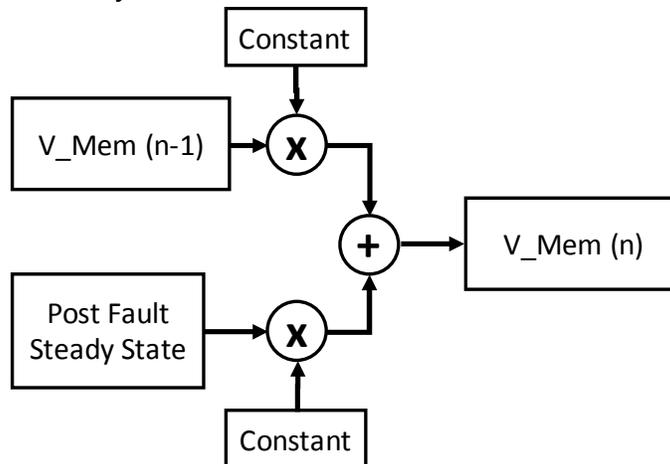


Figure 3 Memory Voltage Block Diagram

Fault resistance is estimated using an approximation provided by Protective Relaying Principles and Applications, shown below in Equation 1 [1], where length is in feet and fault current in primary amps. Applying a factor of two provides an additional safety margin.

$$R_F = \frac{2 \cdot 400 \cdot Length}{I_{F_LL}} \Omega$$

Equation 1 Fault Resistance

The performance of the relay system utilizing voltage memory is analyzed with the assumption that the source voltage is at a value of one per-unit. The voltage memory shown in Figure 3 is implemented with Equation 2 in the SEL-200 series relays [2].

$$VPH1M_k = \frac{1}{16} VPH1_k - \frac{15}{16} VPH1_{k-2}$$

Equation 2 SEL-200 Series Memory Voltage

POTT Scheme Fault Resistance Coverage

The total time delay is needed to calculate final fault resistance coverage because fault resistance coverage will decrease with longer delays. Figure 4 breaks down the multiple factors that add up to the total trip time delay in a typical POTT scheme. Trip time estimates are based on the SEL-421 relay instruction manual [3] and Maximizing Line Protection Reliability, Speed, and Sensitivity [4].

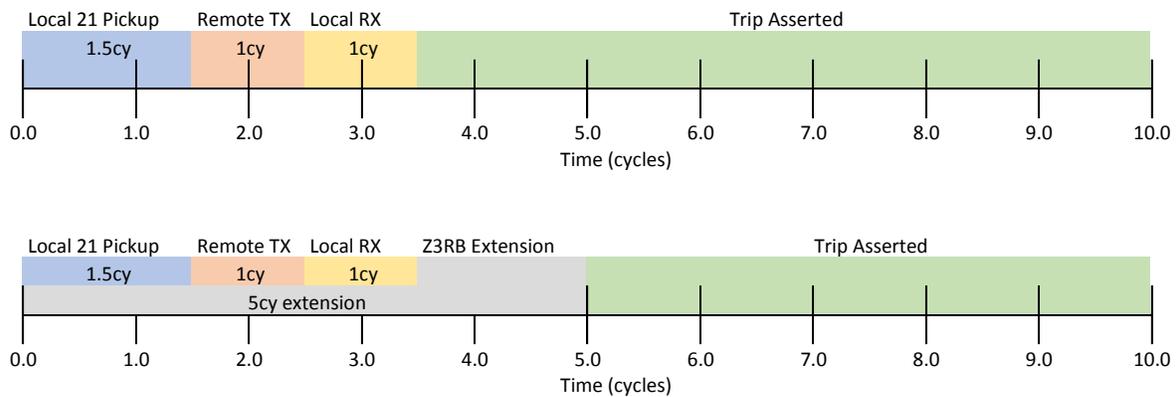


Figure 4 POTT Scheme Time Delays with and without Z3RB

With time delays included, the fault resistance coverage of the system is approximately 0.7 ohms as shown in Figure 5 when the zone 3 blocking logic operates.

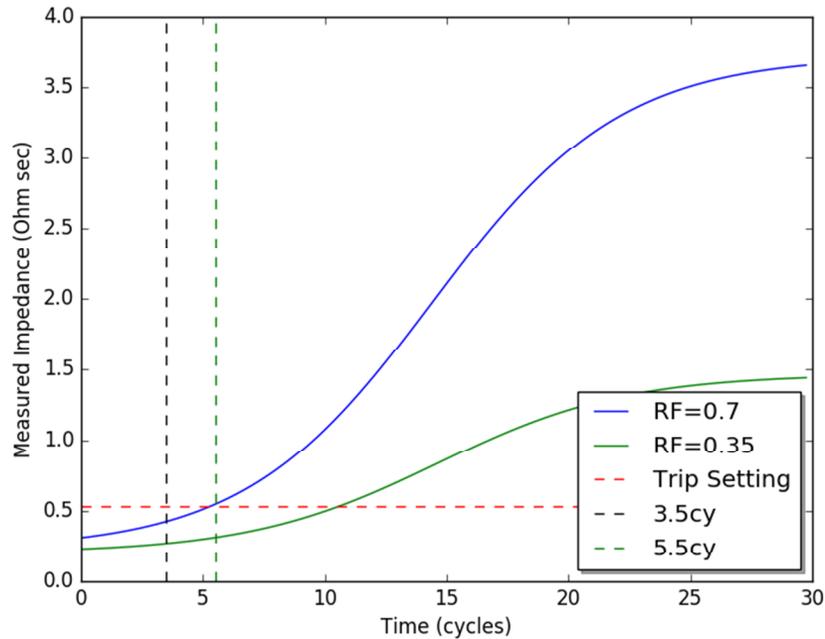


Figure 5 POTT Fault Resistance Coverage

Fault resistance coverage will decrease if the remote end zone 3 picks up prior to a fault, the zone 2 communications assisted trip time delay is increased, or the communications delay increases. Note that an evolving fault at the remote terminal that initially picks up the reverse zone 3 element can cause a significant delay in the total time to trip.

Figure 5 shows the fault resistance coverage falls off towards the steady state value as the reverse block extension timer is increased. This is expected, as the memory voltage will have more time to decay before a trip is initiated given the Z3RB timer is extended.

When Memory Voltage is not Enough

Some systems may still cause issues for a POTT scheme using mho elements. The system used here closely mimics a case that initiated this in-depth look at the total fault resistance coverage. The worst-case fault for this system occurs when a remote bus fault occurs that evolves into a line fault, causing the zone 3 blocking logic to operate. Once the memory voltage has decayed, the zone 2 element will dropout and no longer assert for this fault. This reduction in performance can also occur if the blocking logic dropout time is increased beyond the standard 5 cycle margin, as shown in Figure 5.

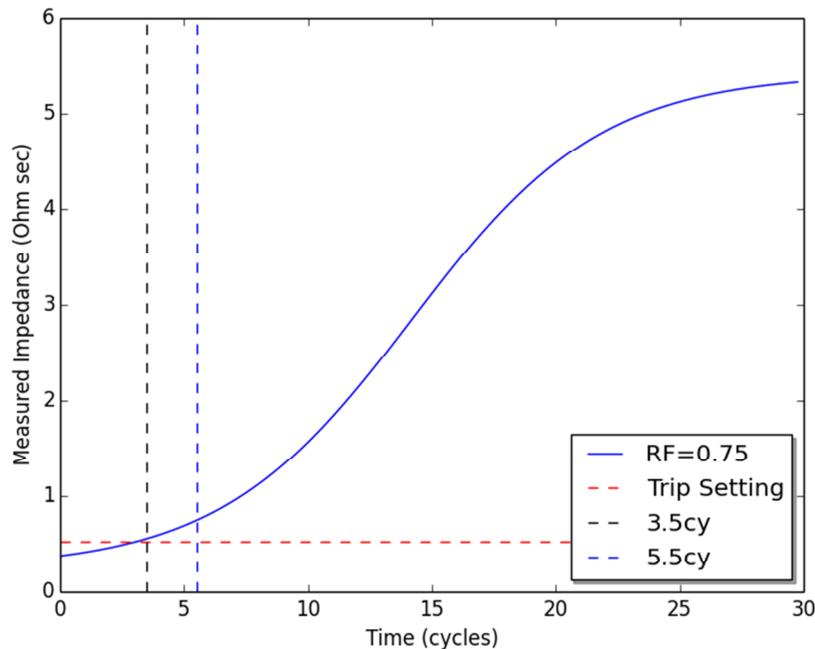


Figure 6 Lack of Fault Resistance Coverage

If this fault clears within 3.5cycles, the POTT scheme will still perform as intended. However, if the time delay exceeds this value, the fault will not be cleared. Some solutions to this problem include:

1. Replace the POTT scheme with line current differential
2. Replace the POTT scheme with a DCB scheme
3. Replace Mho elements with quadrilateral elements.

Solution 1 has the benefit of providing high-speed fault clearing for a variety of faults. However, this solution requires a communications channel that can support the bandwidth and time limitations required for line current differential. If primary and backup relays both share the same high-speed communications system, it may be possible for a single equipment outage to cause loss of high-speed fault clearing.

Solution 2 will increase fault coverage by providing a faster trip and reducing the amount of memory voltage decay before a trip is issued. The communications scheme can be made more dependable by using separate communications systems for primary and backup relaying as only a simple on-off channel is required for the DCB scheme. These advantages come at the cost of miscoordinated tripping on out of zone faults when the communications scheme fails to operate.

Solution 3 provides increased fault resistance coverage while still maintaining the security of the POTT scheme. This solution also allows for a simple communications scheme to be used, making it easier to implement separate primary and backup communications systems. This scheme does not have the security issues of a DCB scheme, but will fail to operate if the communications channel fails.

The proper solution depends on the required fault resistance coverage, type of communications scheme employed, and requirements for primary and backup relay redundancy.

Conclusion

Performance of memory polarized elements can vary greatly depending on the time required to assert a trip signal. To maintain adequate relay performance, this time dependent response should be considered when selecting time delays.

Bibliography

- [1] T. D. J. Blackburn, Protective Relaying. Principles and Applications, Third Edition, Boca Raton, FL: Taylor & Francis Group, 2007.
- [2] I. E. O. Schweitzer, New Developments in Distance Relay Polarization and Fault Type Selection, Pullman, WA: Schweitzer Engineering Laboratories, Inc., 1991.
- [3] Schweitzer Engineering Laboratories, Inc., SEL-421-4, -5 Relay Protection and Automation System Instruction Manual, Pullman, WA: Schweitzer Engineering Laboratories, Inc.
- [4] H. J. Altuve, K. Zimmerman and D. Tziouvaras, Maximizing Line Protection Reliability, Speed, and Sensitivity, Pullman, WA: Schweitzer Engineering Laboratories, Inc., 2016.

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Appendix

The python code that was used to generate the figures in this paper can be found at the following location: <http://github.com/JLHulme/MhoPerformance>