Bus Protection Fundamentals

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Bus Protection Requirements

- High bus fault currents due to large number of circuits connected:
  - CT saturation often becomes a problem as the CT may not be sufficiently rated
  - Large dynamic forces associated with bus faults call for fast clearing times in order to reduce damage due to a bus fault
  - High incident energy/arc flash

- False trip by bus protection may create serious problems:
  - Service interruption to a large number of customers (distribution and sub-transmission voltage levels)
  - System-wide stability problems (transmission voltage levels)
  - With both dependability and security important, preference is always given to security
Bus Protection Techniques

- Interlocking schemes
- Overcurrent (unrestrained, unbiased) differential
- Overcurrent percent (restrained, biased) differential
- High-Impedance schemes
- Low-Impedance microprocessor-based schemes
The Over-Current Problem

Diagram showing electrical systems with labels such as Gen, Bus1, Bus2, Bus3, F60-1, F60-2, F-1, F-2, F-3, F-4, CT1, CT2, F60-1, and F60-2. The text mentions downstream fuse FS1 and upstream and downstream relay numbers (52-1, 52-2). Additionally, it includes a graph with fault current at 11 kV and time to operate (s).
The Over-Current Problem
The CT Problem
The CT Problem

Fault with full DC offset:
The Re-Configurable Bus Problem
Interlocking Schemes

- Blocking scheme typically used
- Short coordination time required
- Practically, not affected by CT saturation
- The blocking signal could be sent over communications ports
- This technique is limited to simple one-incomer distribution buses
Overcurrent (unrestrained) Differential

- Differential signal formed by summation of the bus currents
- CT ratio matching may be required
- On external faults saturated CTs yield spurious differential current
- Time delay used to cope with CT saturation
- Instantaneous (unrestrained) differential OC function useful on integrated microprocessor based relays
Percent (restrained) Differential

- Percent characteristic used to cope with CT saturation
- Restraining signal can be formed in a number of ways
- No dedicated CTs needed
- Protection of re-configurable buses possible

\[ I_{DIF} = |I_1 + I_2 + \ldots + I_n| \]

\[ I_{RES} = |I_1| + |I_2| + \ldots + |I_n| \]

\[ I_{RES} = \max(|I_1|, |I_2|, \ldots, |I_n|) \]
Sloped Diff & CT Saturation Problem

differential

t₀

t₂

restraining
Sloped Diff & CT Saturation Problem
Low Impedance Bus Protection

- No need for dedicated CTs
- High Internal CT ratio compensation
- Advanced algorithms supplement the percent differential protection function making the relay very secure
- Protection of re-configurable busbars becomes easy as the dynamic bus replica (bus image) can be accomplished without switching physically secondary current circuits
- Integrated Breaker Fail (BF) function can provide optimal tripping strategy depending on the actual configuration of a busbar
- Distributed architectures replace CT wires with fiber
High Impedance Bus Differential

- $I_1 + I_2 + I_3 + \ldots + I_n = I_d = 0$
  The vectorial sum of all primary currents in and out of the bus equals zero

- $i_1 + i_2 + i_3 + \ldots + i_n = i_d = 0$
  The vectorial sum of all CT secondary currents (assuming same CT ratio and no CT saturation) in and out of the bus equals zero

- $v_1 + v_2 + v_3 + \ldots + v_n = v_d = 0$
  The vectorial sum of all voltages induced on all CT secondary windings during normal load or external fault (no CT saturation) equals zero
High Impedance Bus Protection

• Fast, secure and proven

• Require dedicated CTs, preferably with the same CT ratio. Cannot handle nicely inputs from CTs set on different taps.

• Input from not fully distributed CT winding creates danger for the equipment, because of inducing very high voltages – autotransformer effect

• Can be applied to small buses

• Depending on bus internal and external fault currents, they may not provide adequate settings for sensitivity and security

• Cannot be easily applied to re-configurable buses

• Require a voltage limiting varistor capable of absorbing significant energy

• Does not provide benefits of a microprocessor based relay (e.g. metering, monitoring, oscillography, breaker fail)
Thank You

Questions?