BUILDING A WORLD OF DIFFERENCE

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FAULT COVERAGE OF MEMORY POLARIZED MHO ELEMENTS WITH TIME DELAYS

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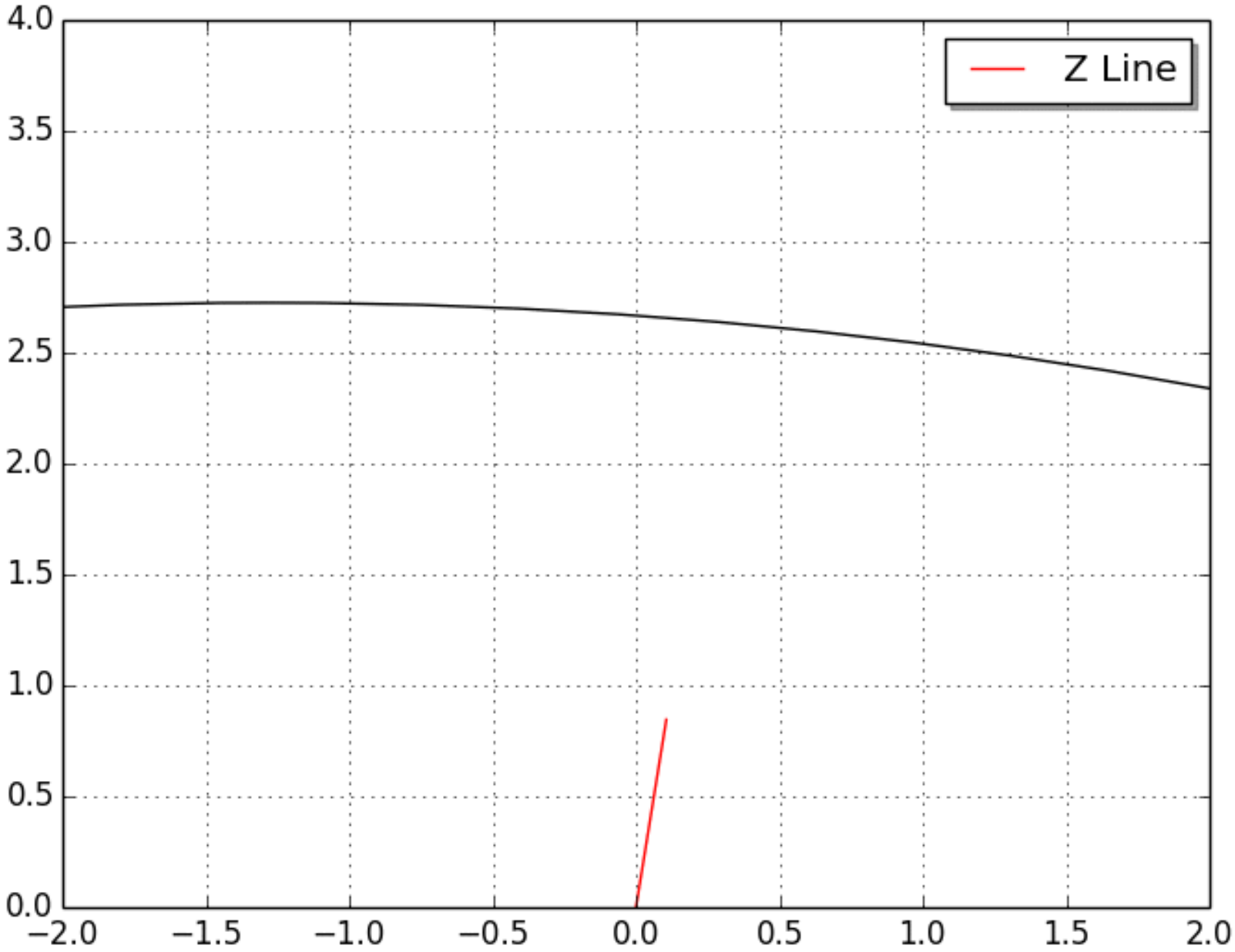
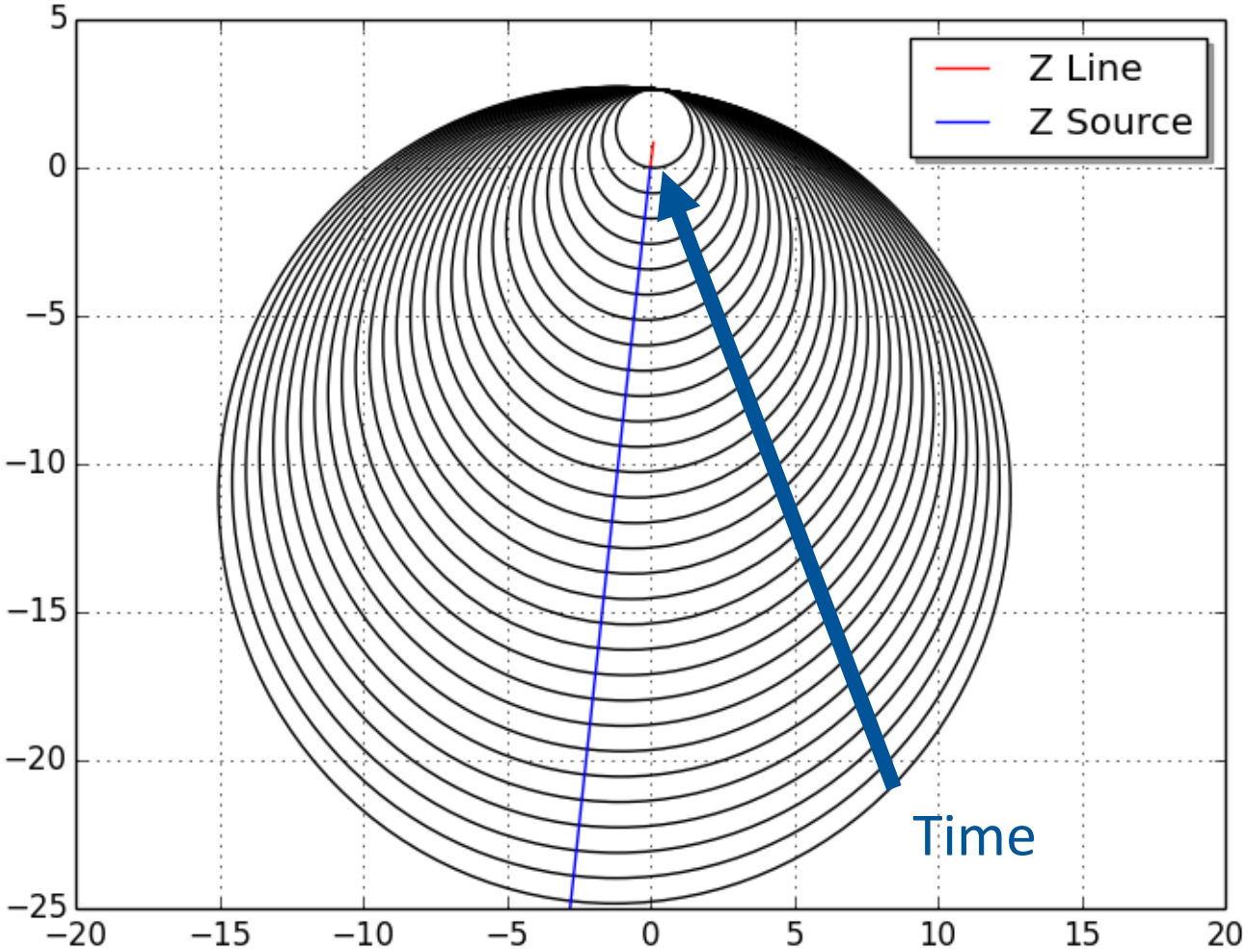
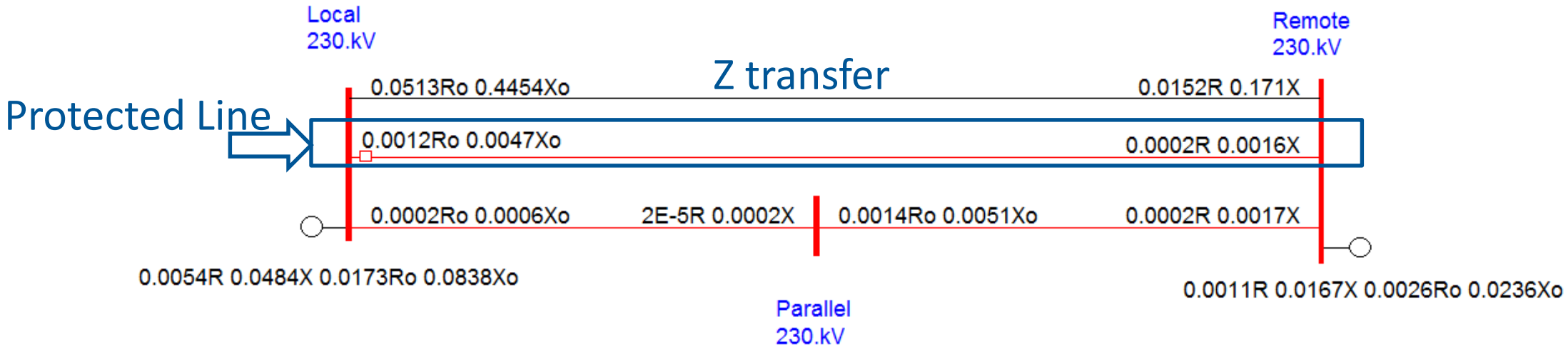

Z Line
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
−2.0
−1.5
−1.0
−0.5
0.0
0.5
1.0
1.5
2.0


Z Line
Z Source
Time
5
0
−5
−10
−15
−20
−25
−20
−15
−10
−5
0
5
10
15
20

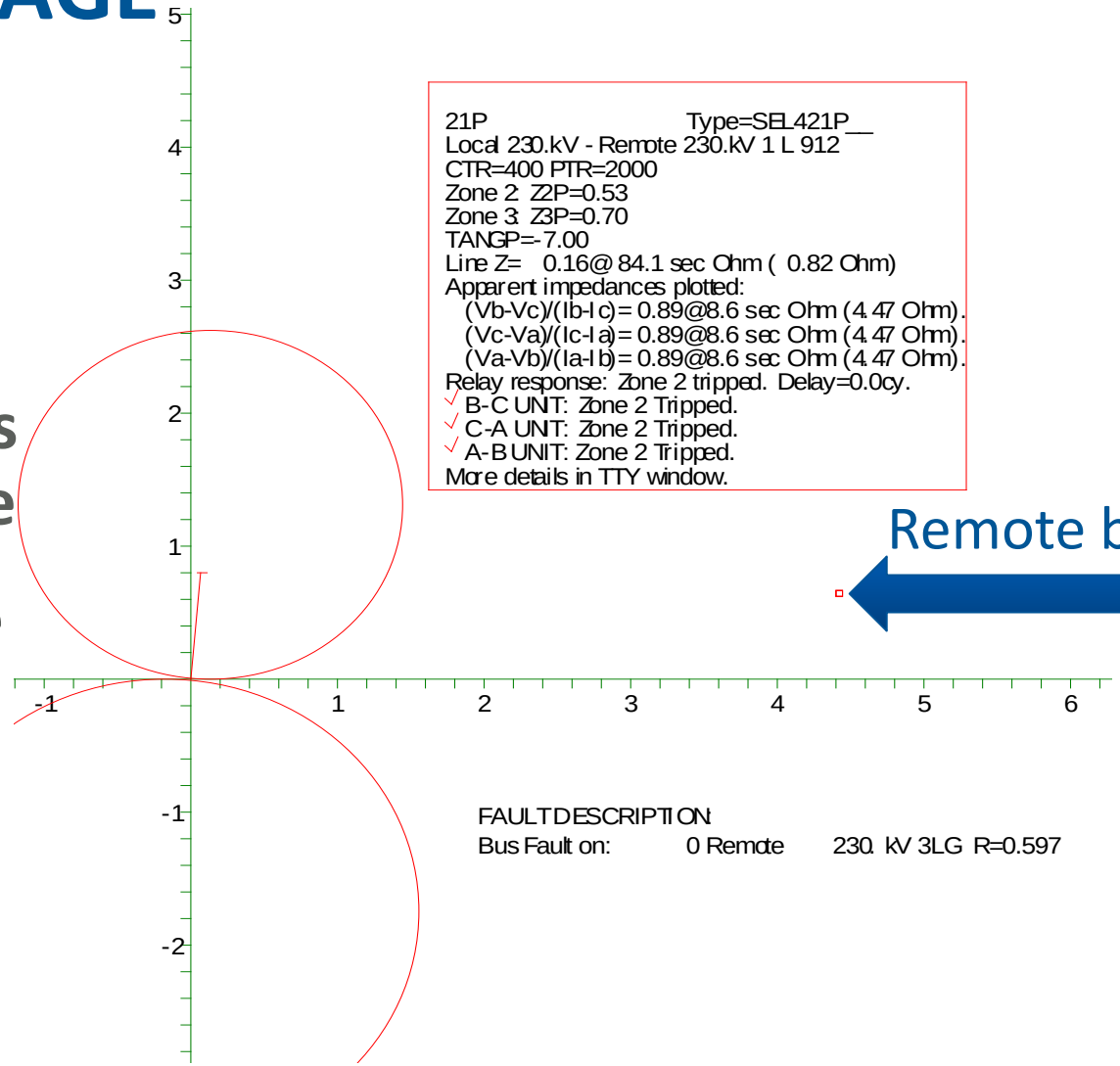
SYSTEM DESCRIPTION



- 230kV system with a series of short lines near generation
- Worst case trip time needs to be < 10 cycles
- Parallel section shares towers with protected line

ZONE 2 FAULT COVERAGE

- Zone 2 mho circle fault coverage is very small
- 230kV phase spacing causes a significant fault resistance
- Plotted fault is well outside the Mho circle

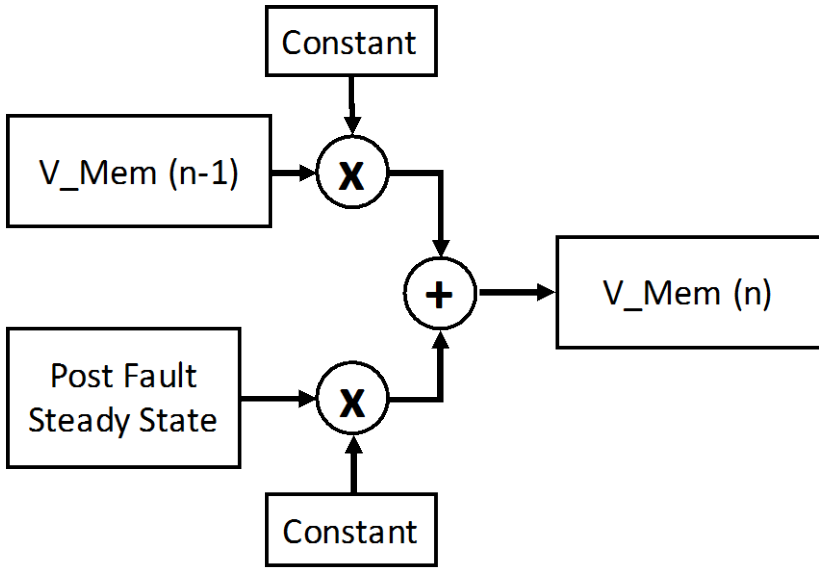


ACTUAL PERFORMANCE

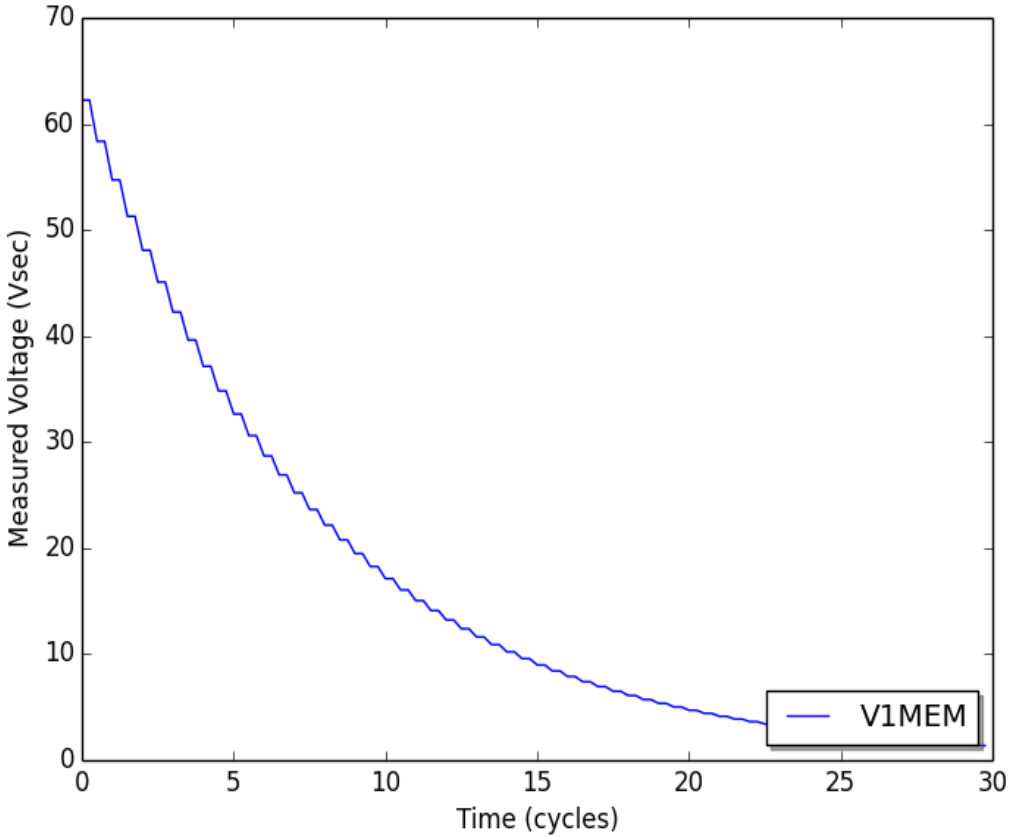
- **Even with the fault outside the mho circle ASPEN indicates a trip**
  - This is due to the memory voltage
  - The trip indication only lasts for a limited time
- **To find this margin the actual relay element was simulated in python**

HOW THE MEMORY VOLTAGE IS CALCULATED

- For the relay used in this case:
- $VPH1M_k = \frac{1}{16}VPH1_k - \frac{15}{16}VPH1_{k-2}$
- This decay allows the trip to assert for a period of time

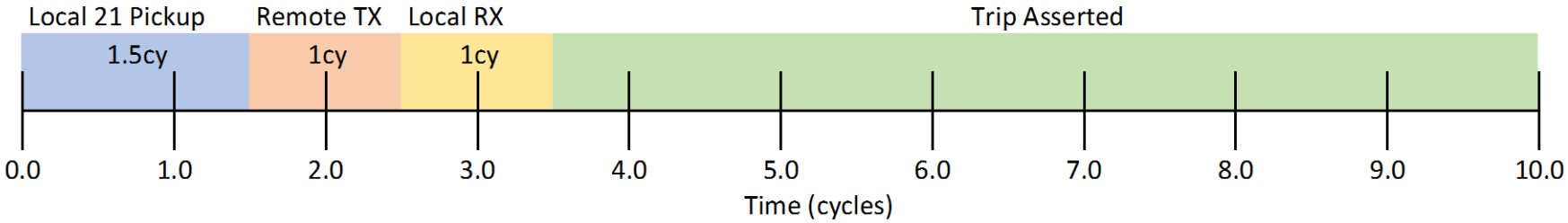


VOLTAGE RESPONSE



- Fault case: Remote bus fault with resistance
- The voltage has a time constant of 4 cy and decays to half the original value in ~6cy

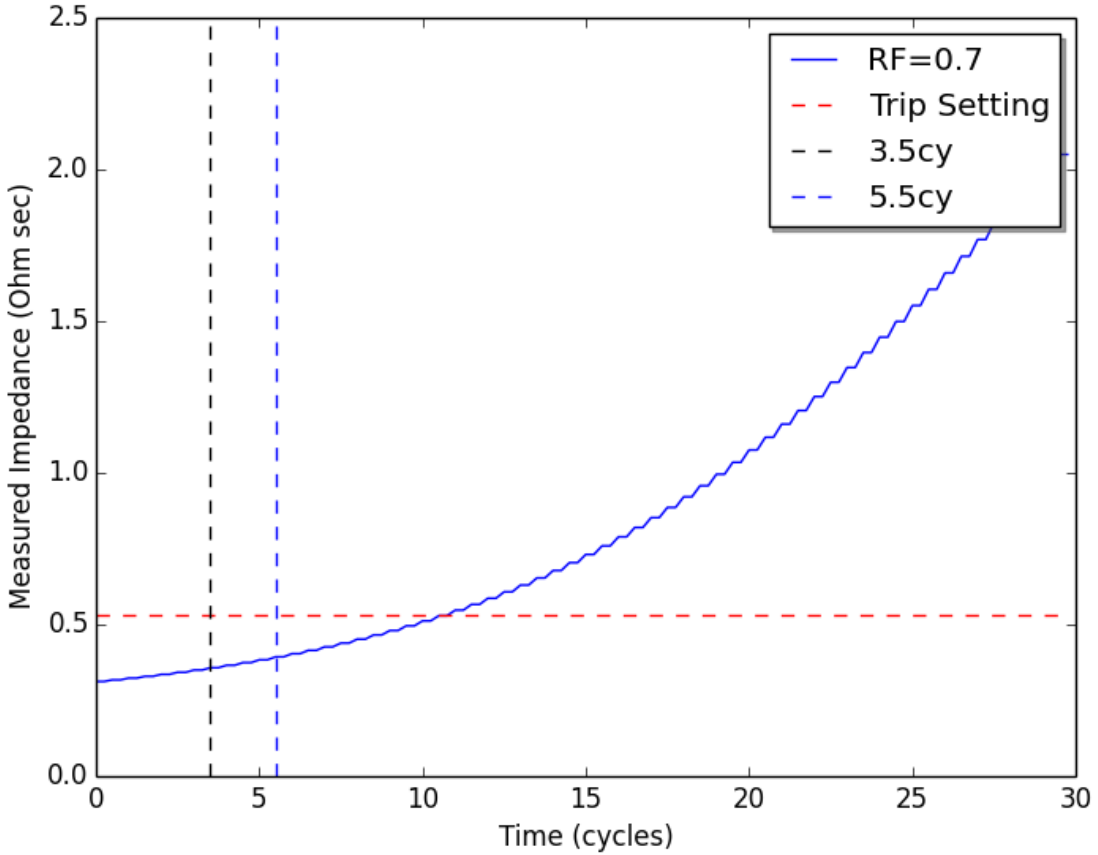
TIME DELAYS

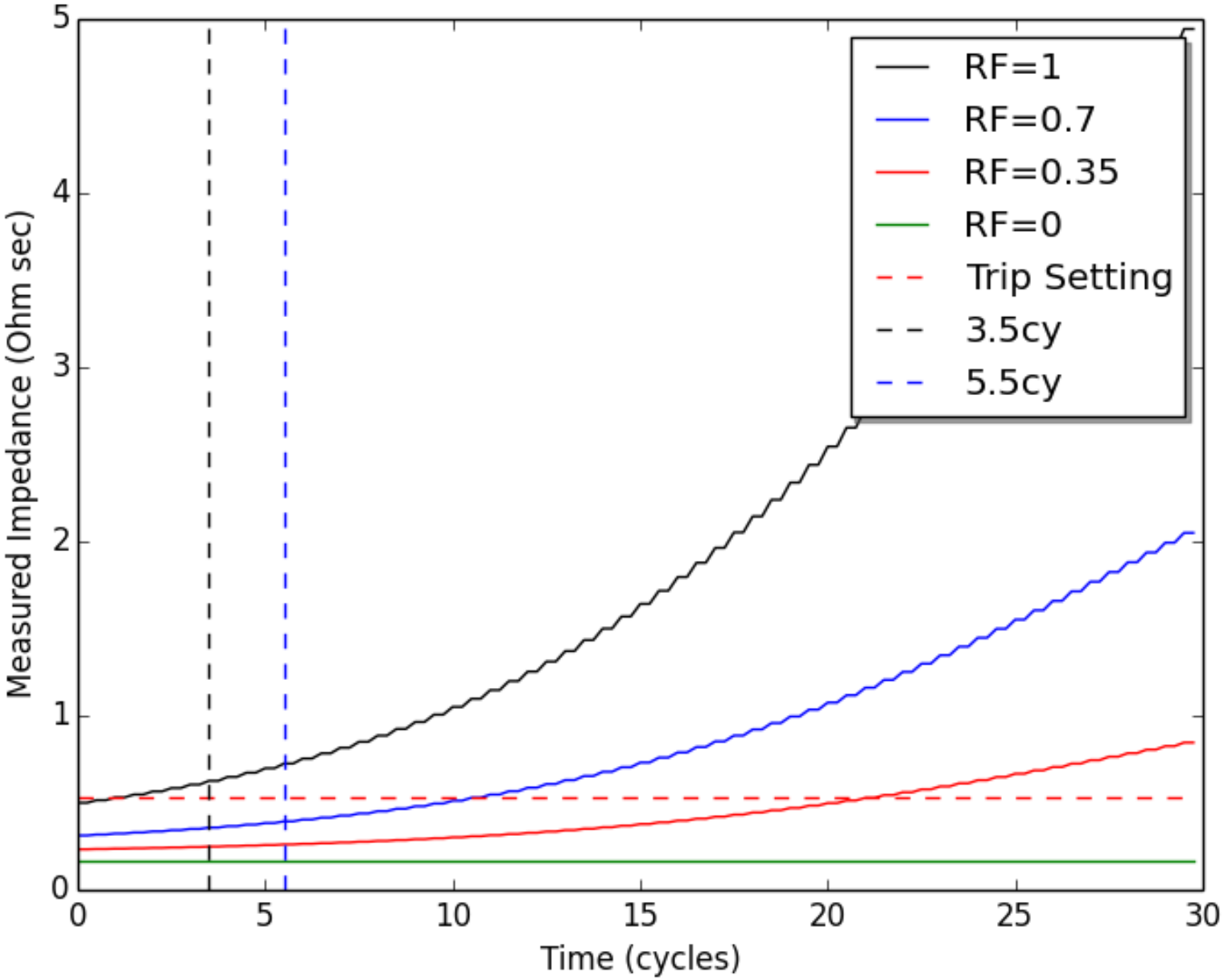


- Fiber communications scheme estimated time delay
- 3.5cycles
- Should allow for operation with a margin of 2cycles

MHO ELEMENT RESPONSE

- Relay will assert trip for 10cy
- That is the maximum POTT operate time
- Slower and a terminal could stop asserting trip
- For this case the estimated worst case fault clears
- RF is simulated fault resistance





Response with increasing resistance

WHEN THIS IS AN ISSUE

- Delayed clearing is unacceptable, cannot wait for step distance to trip
- Coordination and other considerations restrict POTT scheme reach
- Communications schemes with longer delays
- Phase spacing is large (higher arc resistance)
- Fault currents are low (higher arc resistance)

POTENTIAL SOLUTIONS

- **If fault resistance coverage isn't enough and POTT zone can't be increased:**
  - Add a line current differential
  - Replace POTT with DCB if dependability is required over security
  - Check if quad elements are a better fit

END

https://github.com/JLHulme/MhoPerformance
Link can be found in the paper