Enhanced Fault Location Method for Shunt Capacitor Banks

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Outline

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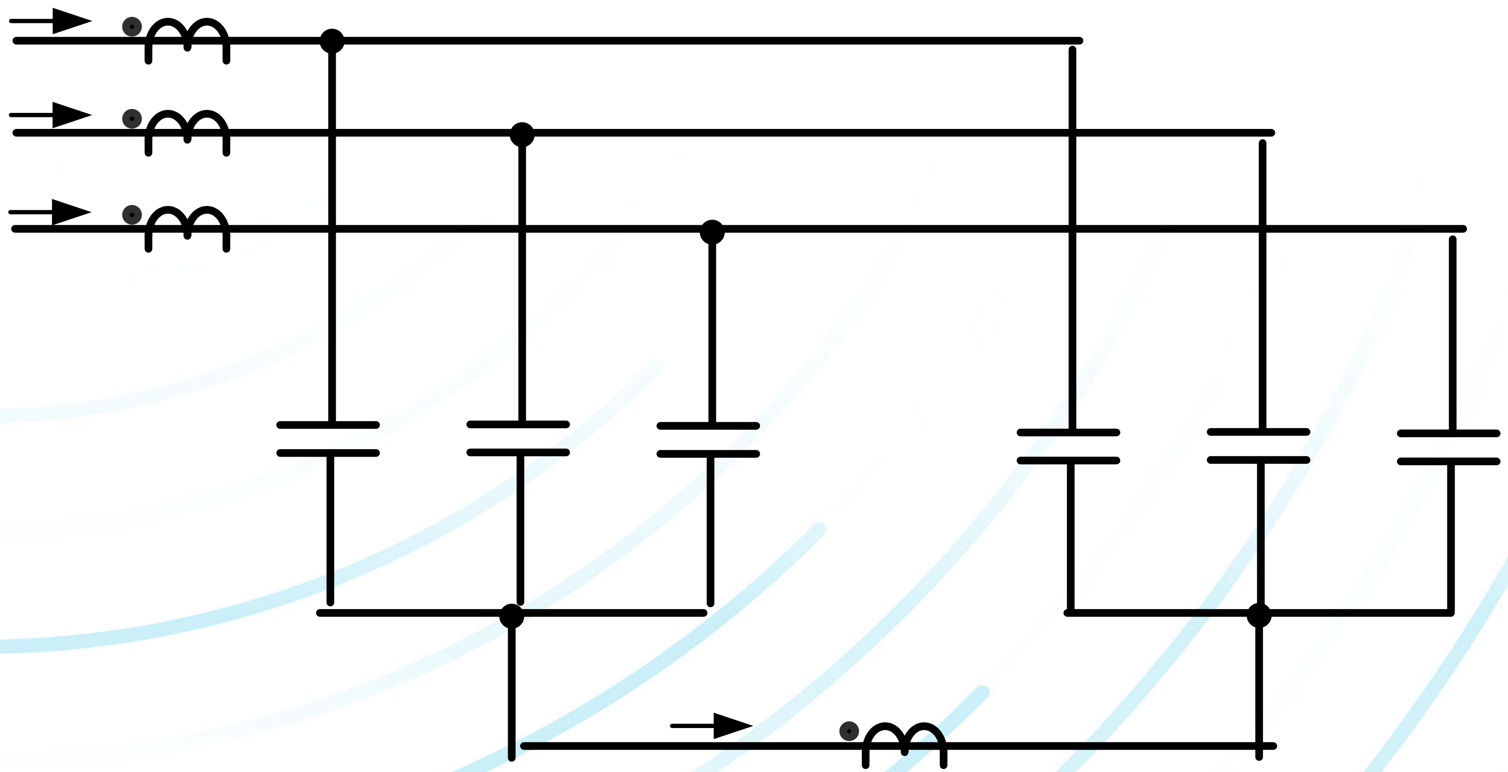
- Enhanced fault location method
  -Ungrounded double wye banks
  -Grounded double wye banks
- The new method flowchart and data for application setting
- Simulation model and method evaluation
- Conclusions

Introduction

- Over voltages, over temperature, manufacturing defects can cause internal failures of capacitor units
- The search of the faulty capacitor can in large high voltage capacitor bank can take significant time and should be reduced to expedite the repair process
- Fuseless and internally fused designs do not have any visual indication for the failures
- By using fault location algorithms the search space can be reduced to 1/6 in double wye capacitor banks
- Detecting consecutive and ambiguous failures, live reporting of number of failed elements helps for preventive maintenance and thus reducing unscheduled outages.

Ungrounded banks

- DOUBLE WYE UNGROUNDED BANKS



Ungrounded banks

- Neutral current can be written in terms of left section currents using current division:

$$I_N = K_A \cdot I_A + K_B \cdot I_B + K_C \cdot I_C; \quad K_p = \frac{X_p^r}{X_p^l + X_p^r}; \quad p : A, B \; or \; C$$

A compensated quantity is derived by subtracting the before failure from after failure neutral current in each phase

$$I_N^{Comp} = \left(K_{Af} - K_A\right) \cdot I_A$$

- This comes to a phase angle balance equation (basis for decision making)

$$\angle I_N^{Comp} = \angle I_A - \angle\left(X_A^l - X_{Af}^l\right)$$

Reference Phasor

Ungrounded banks

- The current is written in terms of symmetrical components to reduce the number of unknowns:

$$I_N = K_1 \cdot I_1 + K_2 \cdot I_2$$

$$K_1 = \frac{I_1^* \cdot I_N - I_2 \cdot I_N^*}{|I_1|^2 - |I_2|^2}; \qquad K_2 = K_1^*$$

Self-tuning and Auto-setting equation

- To make phase comparison adjustable for both internally fused and fuseless bank we incorporate a sign factor

$$I_N^{Comp} = K_{sg} \cdot \left(I_N - (K_1 \cdot I_1 + K_2 \cdot I_2)\right)$$

Ungrounded banks-bank types

- For fuseless SCBs:

$$K_{sg} = \begin{cases} +1 & \mathit{Left\ Section\ Evaluation} \\ -1 & \mathit{Right\ Section\ Evaluation} \end{cases}$$

- For internally fused SCBs:

$$K_{sg} = \begin{cases} -1 & \mathit{Left\ Section\ Evaluation} \\ +1 & \mathit{Right\ Section\ Evaluation} \end{cases}$$

- Separate left section and right section settings for banks with different number of elements/strings in left and right sections

$$\frac{dI_N}{dX_A^l} = \frac{-X_A^r}{\left(X_A^l + X_A^r\right)^2} \cdot I_A; \qquad \frac{dI_N}{dX_A^r} = \frac{X_A^l}{\left(X_A^l + X_A^r\right)^2} \cdot I_A$$

Ungrounded banks - sensitivity

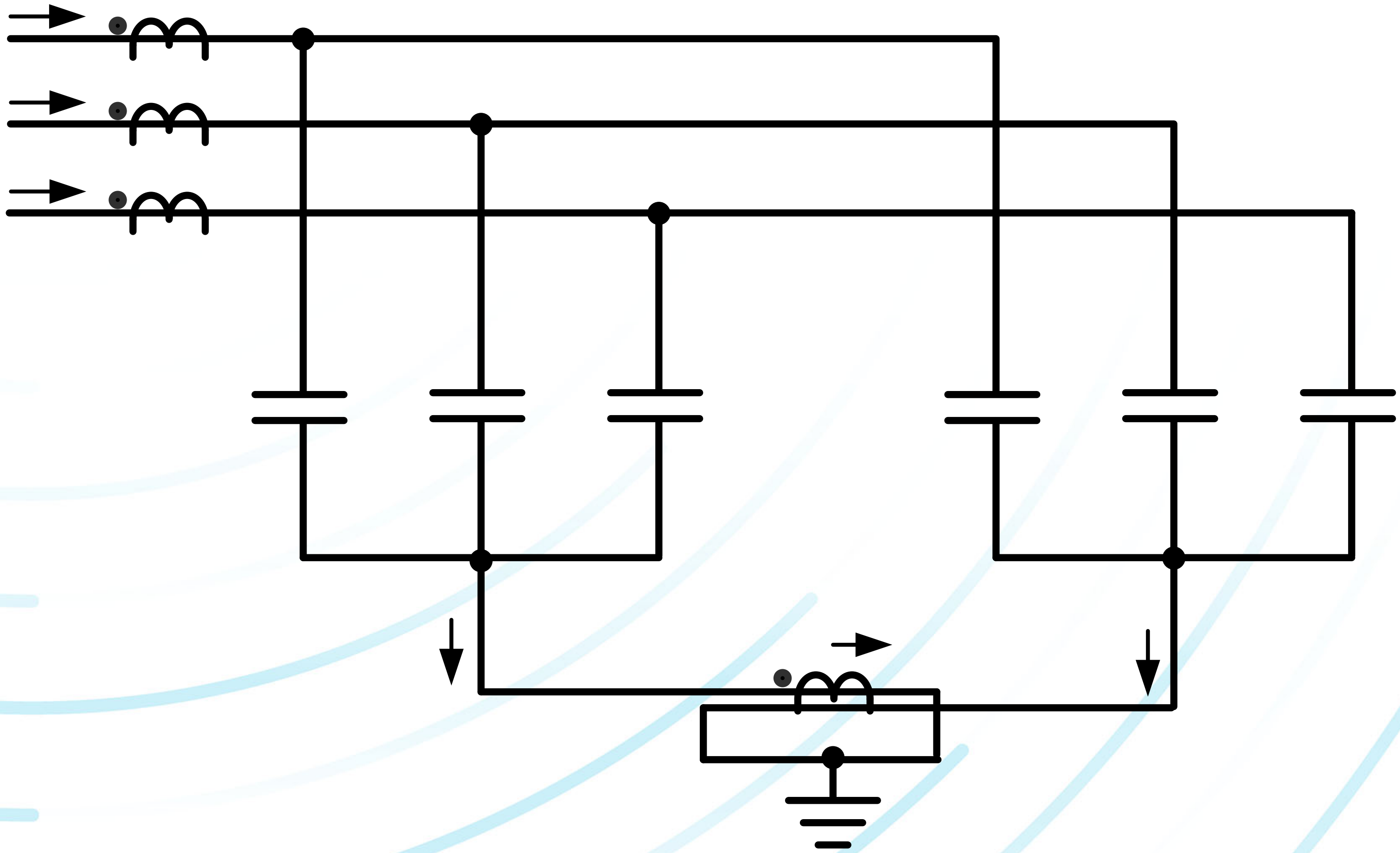
- Suppose the left and right section rated reactance values are related as $X^r = K_x \cdot X^l$, then we have:

$$\Delta I_N(pu) = \begin{cases} \Delta X_A^l(pu) \cdot \dfrac{K_x}{(K_x + 1)^2} & Left\ Section\ Setting \\ \Delta X_A^r(pu) \cdot \dfrac{K_x}{(K_x + 1)^2} & Right\ Section\ Evaluation \end{cases}$$

- Expected change in the neutral current for a single element failure can be used as a base to estimate number of failed elements

Grounded banks

- DOUBLE WYE GROUNDED BANKS



Grounded banks

- Neutral current would be through window CT measuring vectorial difference
- Zero sequence current coefficient is sum of the phase k-factors (likely to be close to zero)

$$K_p = \frac{X_p^r - X_p^l}{X_p^l + X_p^r}; \qquad p : A, B \; or \; C$$

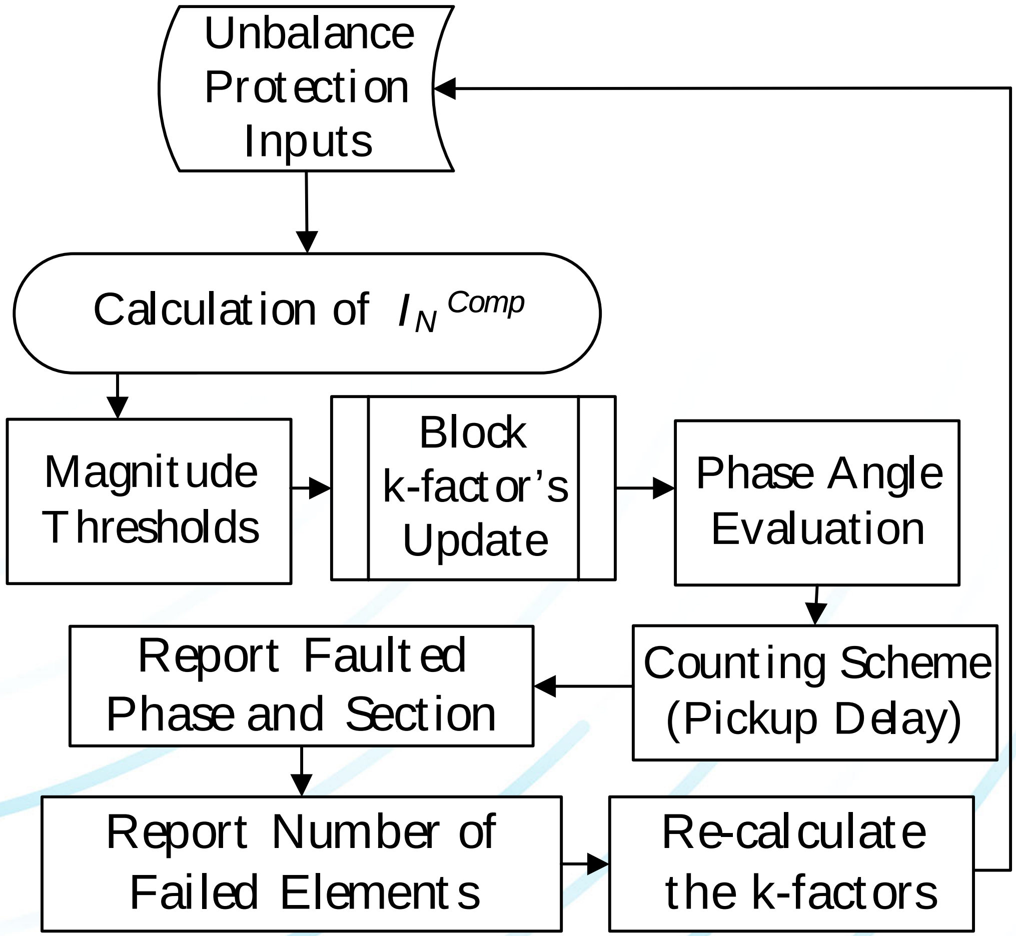
- The zero sequence current impact could be neglected:

$$I_N = K_1 \cdot I_1 + K_2 \cdot I_2$$

- Detection of number of failed elements:

$$\Delta I_N(pu) = \frac{\Delta X}{2}(pu)$$

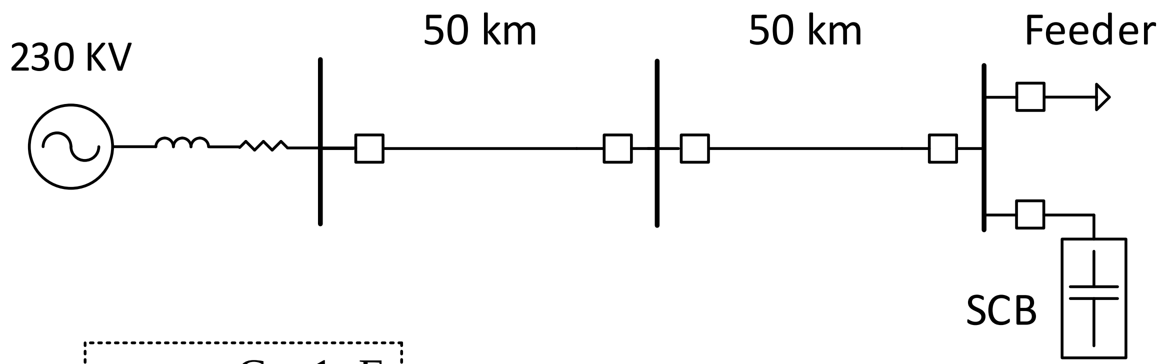
The enhanced method flowchart



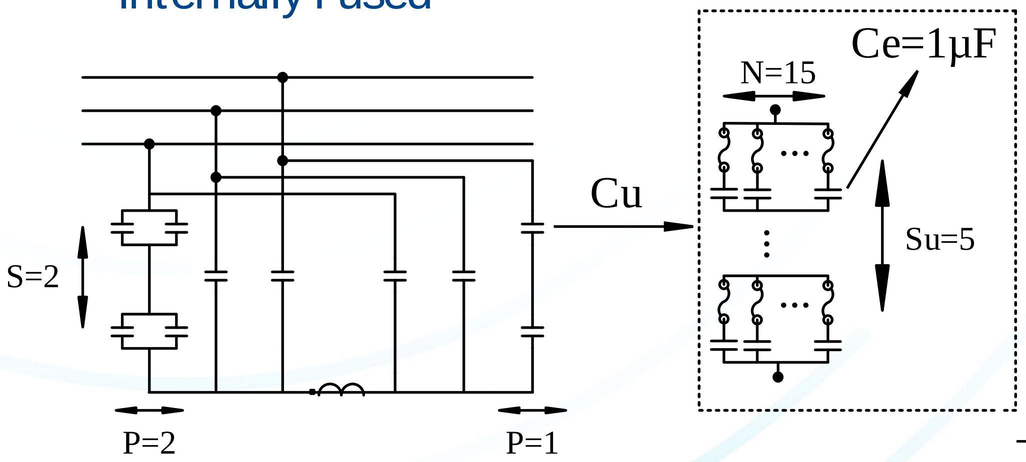
Required data for application setting

- Bank rated current to obtain per-unit the compensated current
- Capacitor element/unit rated capacitance
- Number of parallel and series capacitor elements in each unit and also capacitor units in the bank, both left and right sections
- Whether the bank is Internally fused or fuseless
- Grounded or ungrounded bank
- Failed elements count and count reset

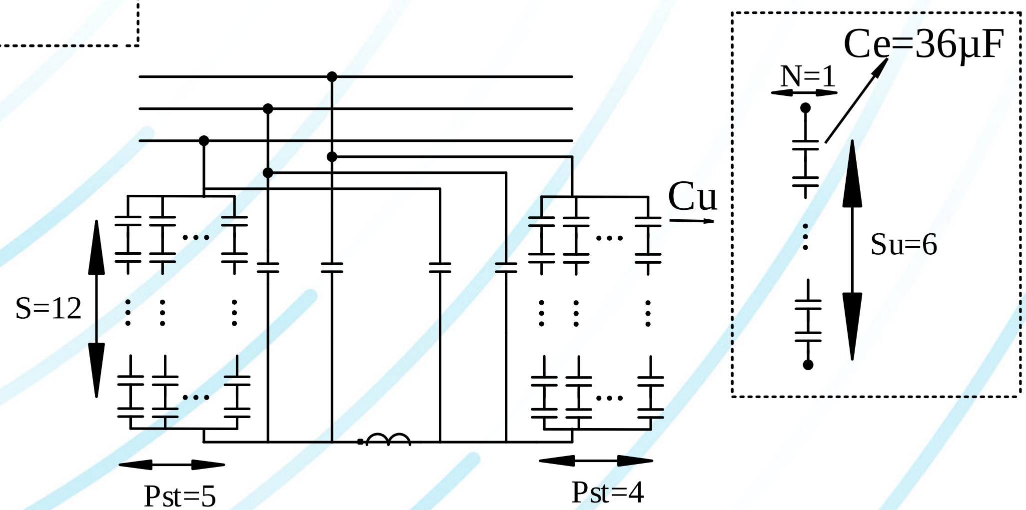
Simulation Model



Internally Fused



Fuseless



PSCAD and Relay models

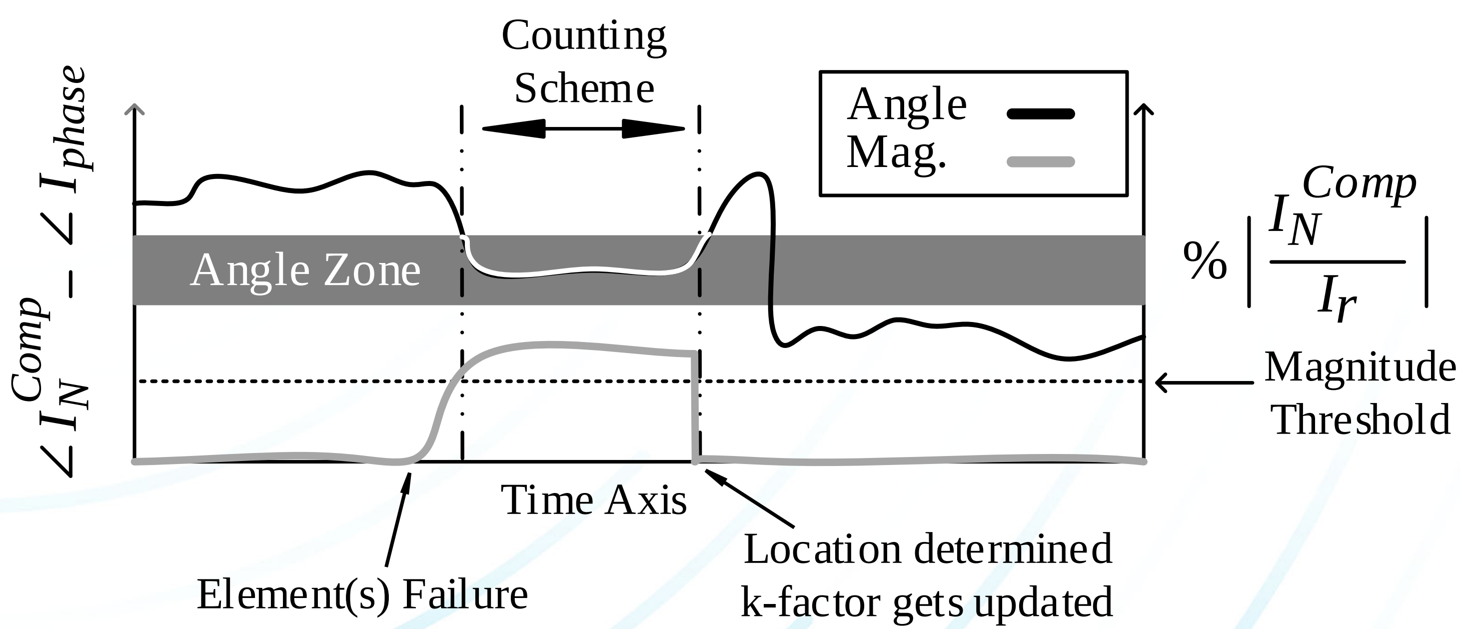
The PSCAD model has considered:

- Unbalance load
- Pre-existing inherent unbalance
- Harmonics
- Measurement noise
- Impact of temperature (could be shading) or aging

The Relay model applies:

- Anti-aliasing filter
- Decaying DC removal
- Full cycle DFT

Decision Making



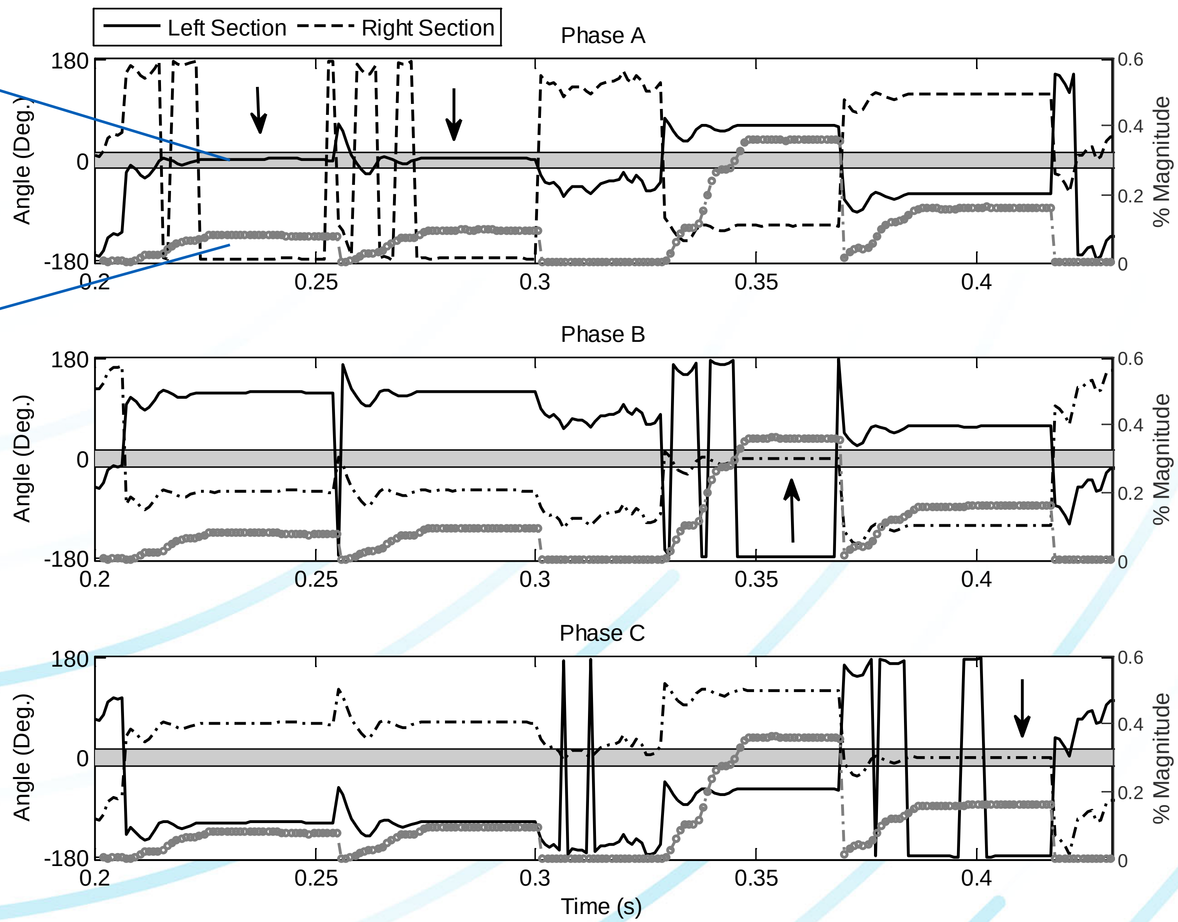
Enhanced Method Evaluation

- Detection of failures in different locations [Ungrounded Bank]

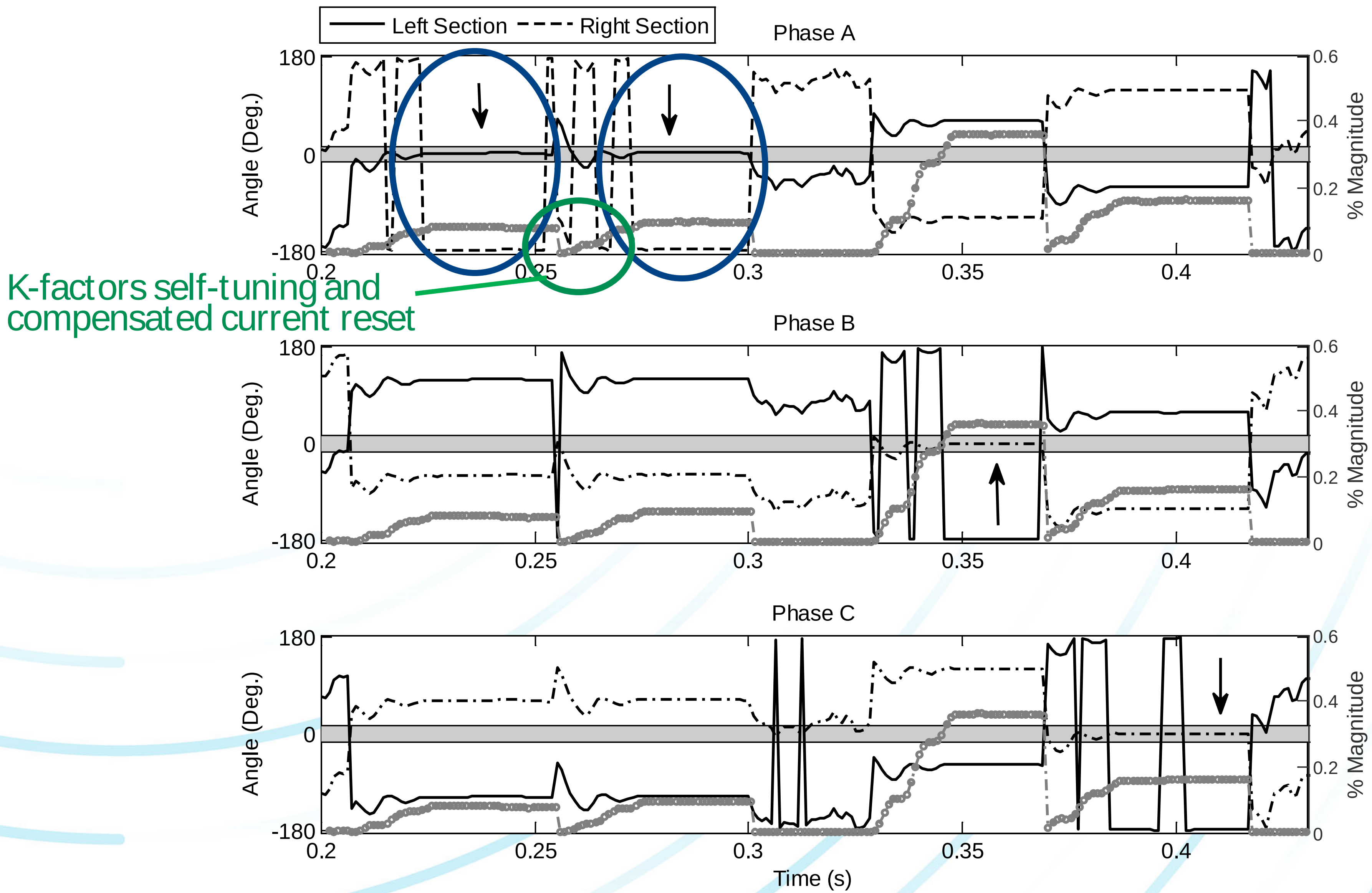
Failures in the order of occurrence: A-Left , A-Left , B-Right , C-Right

Satisfies Angle Criteria

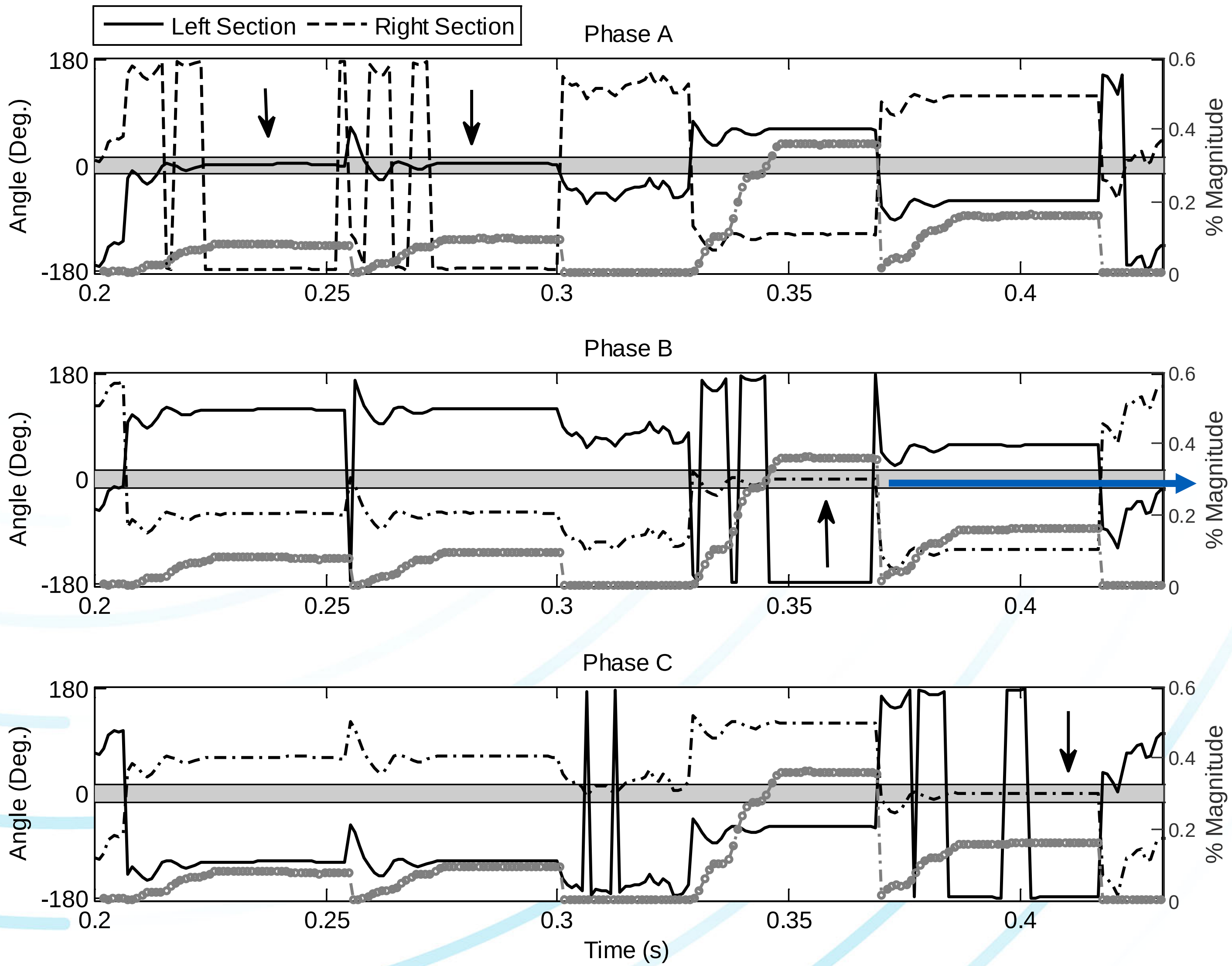
Satisfies Magnitude Criteria



Consecutive failures detection



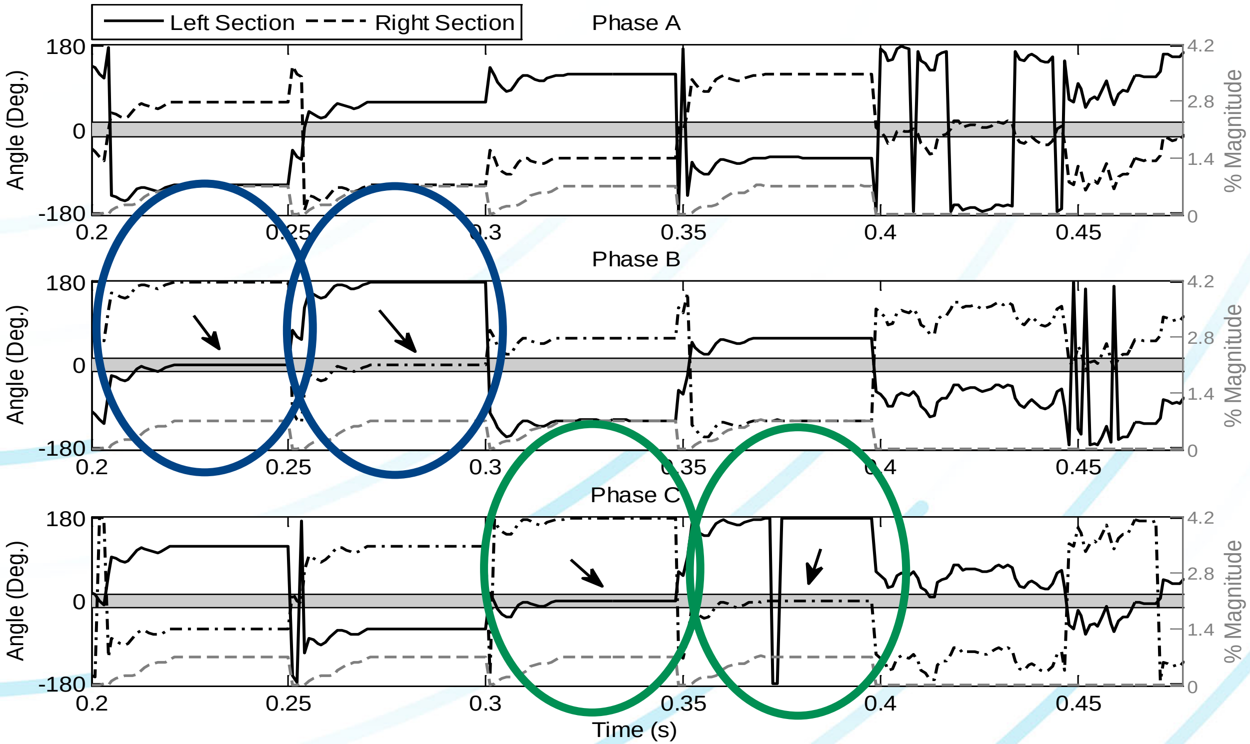
Number of failed elements detection



Note the magnitude because of double element failure

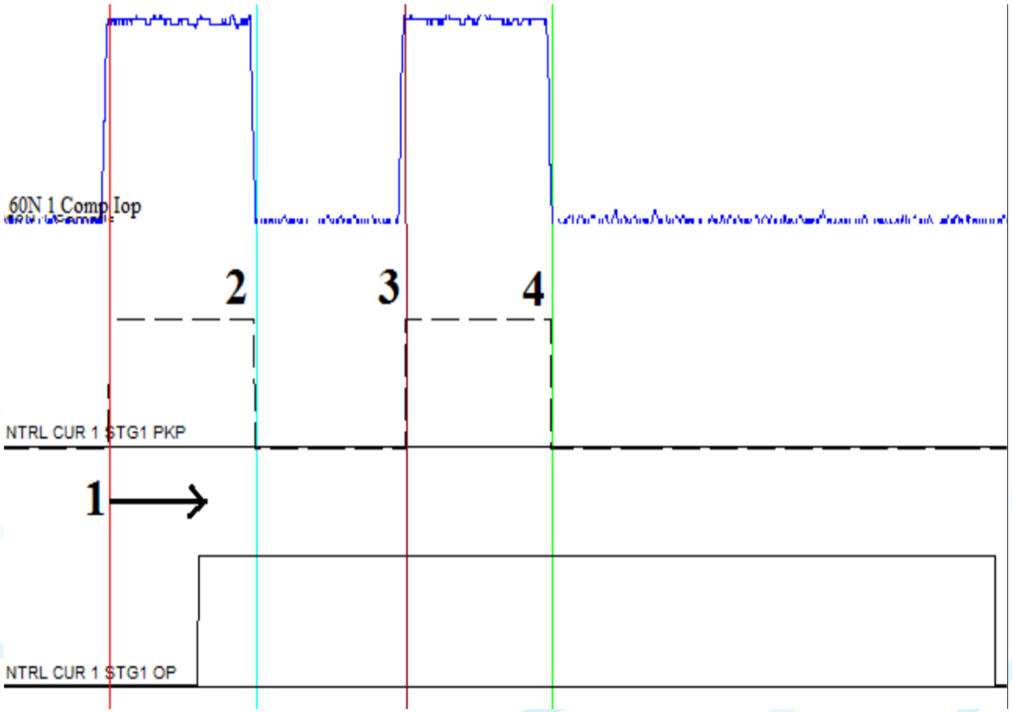
Detection of ambiguous failures

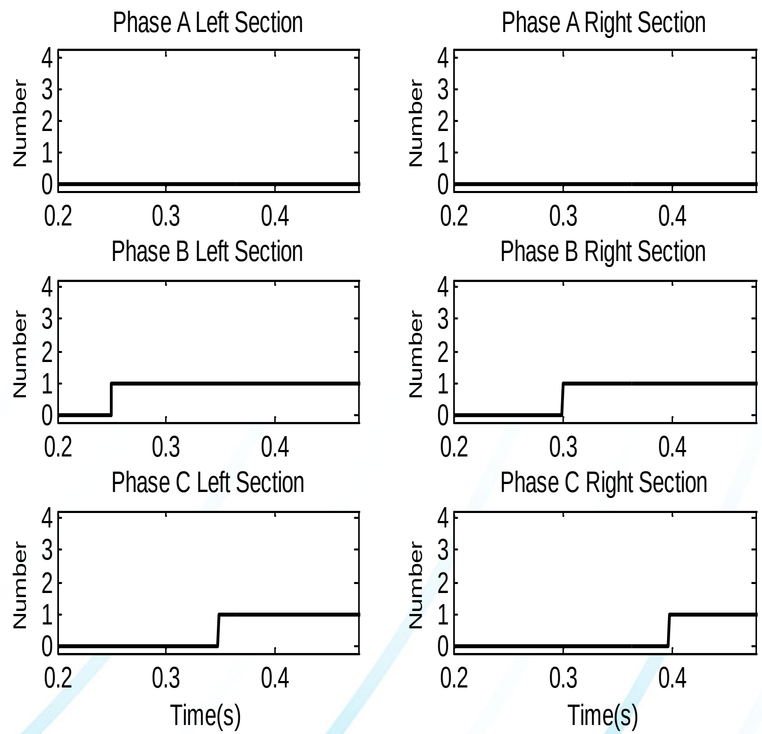
- Failures in the order of occurrence: B-Left , B-Right , C-Left , C-Right
- Right and left section failures in the same phase could seem as a balanced bank to the relay
- Each of them is detected, reported, and self-tuning helps to find the subsequent failures



Detection of ambiguous failure (cont'd)

- Comparing the ambiguous failure case with commercial relay unbalance protection : B-Left , B-Right , C-Left , C-Right

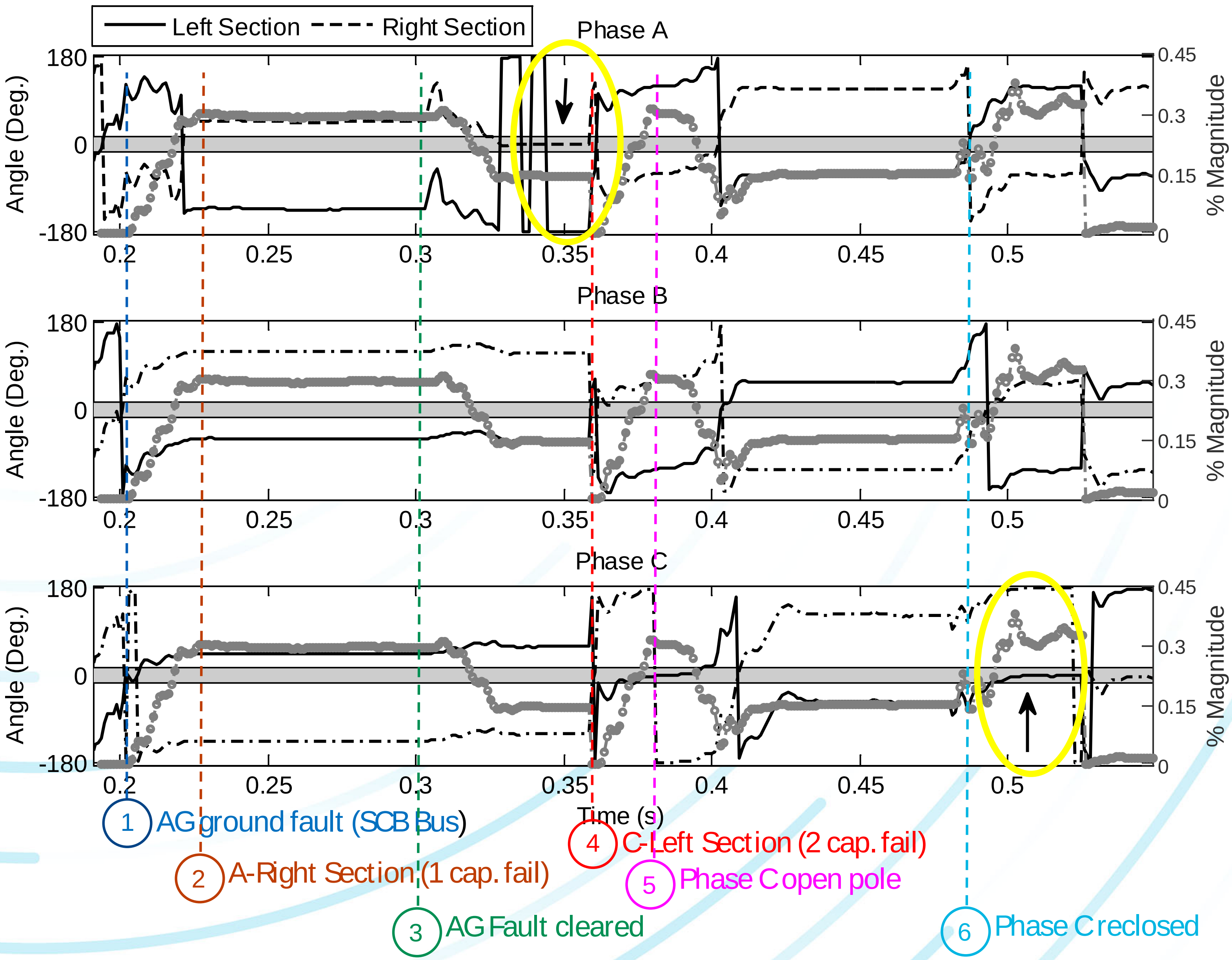




- 1 and 3: STG1 picked up, faulted phase unknown
- 2 and 4: Ambiguous failure not detected, operating quantity reset

- All of the 4 failures are detected and reported accordingly

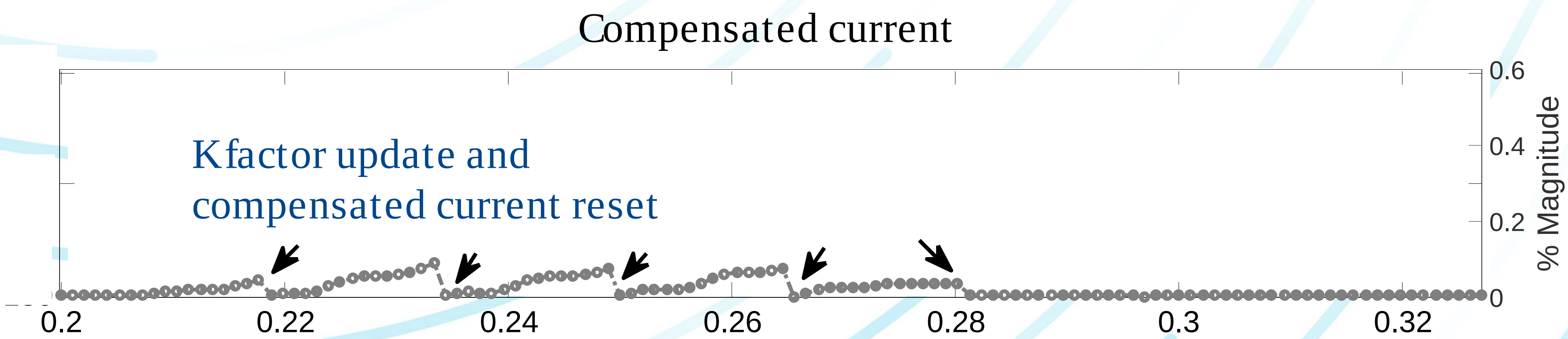
Tolerance to external disturbances



Compensation of gradual changes

- Self-tuning with a regular and pre-determined rate
- Could be set based on the expected rate of change of capacitance for a worst case temperature change, say an hourly update rate for the k-factors to compensate for gradual changes
- Should be blocked for sometime to avoid interference with detecting the faults when an internal failure is suspected

Illustrative scenario with a linear change in capacitance:



Conclusions

- Enhanced fault location method for Internally fused and fuseless double wye capacitor banks is presented to expedite the repair process
- Enhanced fault location method applies self-tuning and auto-setting that result in:
  - Detecting consecutive failures
  - Detecting ambiguous failures
  - Compensating for gradual capacitance changes
  - Compensating for errors due to the CTs by initial setting (commissioning process)
- Enhanced fault location method allows discriminating capacitor elements failures per each phase in left or right section of the double-wye bank even when sections have different capacitance.

Conclusions

- Both compensated neutral current magnitude and angle are used to detect capacitor element failures, making method robust even during external disturbances simultaneously with internal failures.
- Method is immune to external disturbances, noise, bank inherent unbalance, CT inaccuracies.
- Real time report of number of failed elements and location enables quick response for repair

Thank You

Questions?