Does Every Millisecond Really Count – A Comparison of Protection Based Arc Flash Mitigation Techniques

Terrence Smith
Member, IEEE
GE Grid Solutions

Chris Burnette
Member, IEEE
GE Industrial Solutions

Marcelo Valdes
Senior Member, IEEE
GE Industrial Solutions

Abstract – **Much attention has been given to mitigation of the arc flash hazard using various fast protection schemes such as light sensing and differential relaying. This paper examines several techniques and quantifies each technic with model systems. The model system consists of several Thevenin equivalent circuits which produces different maximum fault current levels. These Thevenin equivalent circuits are then examined to build a graph of clearing time verses incident energy. Circuits at 2.3KV, 4KV, 13.8KV, and 0.48KV with fault current ranging from 5KA to 30KA are examined. The paper also discusses light sensing, bus differential, zone interlocking, and time current coordination and how each scheme will affect the incident energy of the model system.**

I. Introduction

NFPA 70E has given the protection engineer a unique opportunity that has never been seen since the inception of the protective relay; the opportunity to not only enhance protection to personnel, but to quantify the enhanced protection. By designing systems that limit the arc flash incident energy, the protection engineer can now design his system around personnel protection as well as equipment protection.

The three primary quantities that influence the arc flash incident energy per the IEEE 1584-2002 Guide model are: maximum fault current, distance to the fault and time to clear the fault. Methods to limit the fault current include: never parallel transformers, addition of line reactors, and increased transformer impedance. Line reactors and increased transformer impedance both negatively impact voltage drop of the system. For these reasons, designs around limiting the fault current by increasing the source impedance have limited merit. The largest factor influencing fault current at industrial facilities is the utility tie transformer impedance. If two identical transformers are placed in parallel, their combined Thevenin impedance will be ½ of the impedance of either transformer alone. This will come close to doubling the fault current on the industrial bus fed from the utility tie transformers and should be avoided so that fault current is limited.

The second way an engineer can influence the arc flash incident energy is with distance. As the distance from the arc-flash event grows, the incident energy also decreases. Protection and control designers can influence distance by moving operations outside the arc flash boundary with remote racking of breakers and remote control operations. In the digital age with microprocessor based relays, switchgear HMI, or engineering access computers there is no reason for personnel to operate equipment inside the arc-flash boundary. This is by far the best method to limit personnel exposure because it doesn't rely on equipment working correctly in an arc-flash event. If the arc-flash occurs the personnel are remote from the event.

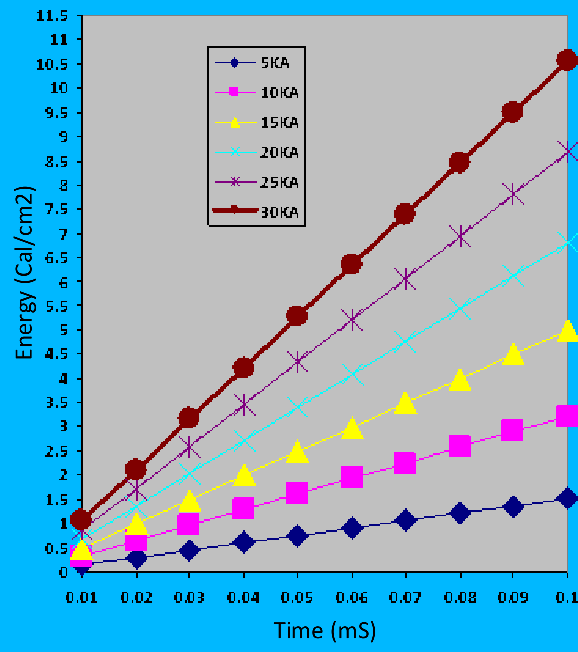

Fig. 1 – 480V Time –vs- Energy Plot

The third method to limit arc-flash incident energy is by influencing the time it takes to clear the fault that has created the arc-flash event. It is this method that this paper explores in detail. Several different protection and control techniques exist for attacking the time to clear. These include: arc-flash relays that sense the light from the event, zone interlocking schemes, bus differential, and reduced energy let through alternate settings. Each of these techniques is a protective relaying technic and only influences the time it takes to signal to an interrupting device. The interrupting device will typically be a circuit breaker with operating times between three and five cycles. In order to quantify the effect of these time limiting solutions a sample system has been built and analyzed with varying voltage levels, fault levels, and clearing times. The system is analyzed is detail in Appendix A. The sample system clearing times were then plotted against the incident energy, with the 480V system shown in Fig 1. Plots for a 13.2KV, 2.3KV, and 4KV system were also built and all four graphs are located in Appendix B. For the systems in Appendix B a 36 inch working distance has been assumed for all of the medium voltage switchgear and an 18 inch working distance has been assumed for the 480V switchgear. A 32mm gap has been assumed for the 480V switchgear, a 102mm gap assumed for the 2.4KV and 4.16KV switchgear and a 153mm gap for the 13.8KV Switchgear.

Using the clearing time verses incident energy graphs in appendix B the influence of the various protection and control schemes can be quantifiable compared.

II. Case Study: Arc-Flash Relay Controlling a Three-Cycle Circuit Breaker.

Several factors influence the total time to clear an arc-flash event. This first factor is the time it takes the protective relay algorithm to operate. Once the algorithm has operated the next factor is the time it takes to close the output contacts on the relay. If tripping is performed with a lockout relay, then the time for that lockout to operate must also be considered. An 86 lockout relay should be avoided if possible, since its increased tripping time and adds a point of potential failure. Lastly, the time required for the breaker to operate and clear the fault must be considered in the arc-flash analysis.

Arc-Flash relays are meant to sense the light caused by the electrical arc in air and operate quickly when the light is sensed. In many instances the light is supervised by some other monitored quantity such as: current, rate of rise of current, or pressure to enhance security and prevent false operations. These quantities are used to supervise the light recognition algorithm because the light recognition algorithm, if left unsupervised, can mis-operate from any event that creates light, such as: camera flash, failing lighting ballasts, or in the case of older air magnetic circuit breakers, the normal arc caused by a circuit breaker during interruption. The recognition of the light from the arc can be very fast, but the method that the algorithm uses to supervise the light can cause the actual operate time of the algorithm to increase significantly. Great care should be taken to understand the actual operate time of the complete relay when doing Arc-Flash studies that mitigate incident energy with arc-flash relays. As an example of the difference in times, a pressure and light algorithm can operate in as little as 4ms while a light supervised with overcurrent can operate in 12ms, and the light supervised by rate of change of current falling between these two extremes.

The time to actually close an output contact can also vary considerably from device to device with times ranging from 100 microseconds for solid state outputs up to 8 milliseconds for some mechanical outputs. For the purposes of this analysis 100 microsecond solid state outputs will be used.

A 4 millisecond algorithm with solid state outputs controlling a three cycle breaker would give an operate time of 54.1 milliseconds while an 8 millisecond algorithm with solid state outputs would give a 58.1 millisecond operate time. If these times are compared to the 4KV and 480V graphs in Appendix B, a comparison of the two algorithms can be developed. With the 480V system and a three phase fault of 25KA the 4ms algorithm would have an incident energy of around 4.8 cal/cm2 while the 8ms algorithm would have an incident energy of around 5.0 cal/cm2. The 4KV system at 25KA fault current would have an energy of 3.4 cal/cm2 for the 4ms algorithm and 3.5 cal/cm2 for the 8ms algorithm.

In these two example systems the method of the algorithm matters because the faster algorithm has lower incident energy, but it does not matter enough to move the incident energy into a separate PPE range. A much more significant factor in the incident energy will most likely be the operate time of the breaker. In this example a three cycle breaker was used, but a five cycle breaker, which is discussed in section VI would significantly impact the incident energy. The better solution may be to replace the older five cycle breaker with a new three cycle breaker.

III. Case Study: Zone-Selective-Interlocking Scheme Controlling a Three-Cycle Circuit Breaker.

In a Zone-Selective-interlocking scheme, the electrically upstream circuit breaker relay has a definite time element that does not need to coordinate with the downstream circuit breaker relays. The non-coordinating element is meant to operate fast for faults between the upstream circuit breaker and downstream circuit breaker. For faults below the downstream circuit breaker, the downstream circuit breaker relay will send a “blocking” signal to the upstream circuit breaker relay which will block the non-coordinating element. Typically, the blocking signal will stop a protective function from operating. In this example, it would stop the fast, non-coordinating element from operating. Alternately, the blocking element could simply slow down the fast element or change the settings group of the protective relay so that the element is effectively stopped or slowed.

To better explain the operation of the zone-selective-interlocking scheme, consider the bus scheme shown in Fig. 2 below. If a fault occurs on one of the feeders off the main bus, the feeder relay 50 element (instantaneous overcurrent) will pick up and send a blocking signal to block the 50 element on the main. If the fault is on the bus between the main and the feeder circuit breakers, the feeder circuit breaker 50 elements won’t pick up and the block signal won’t be sent and the main relay’s instantaneous (50) element operates fast, clearing the fault in minimum time. A key requirement of the zone-selective-interlocking scheme is that the feeders are radial and cannot feed fault current back into the bus that exceed the blocking threshold. If faults on the bus can be feed from the feeders at a current level that exceeds the threshold used for blocking, directional overcurrent sensing becomes necessary and will typically take about half a cycle to one cycle longer to operate. Additionally, normal time coordinated overcurrent elements should be used on the main breaker relays to “back up” the scheme.

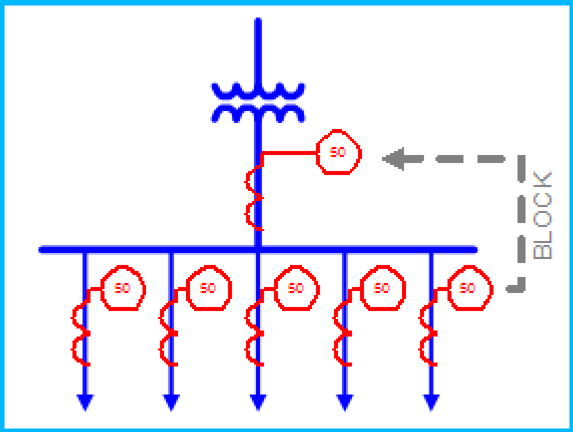

Fig. 2 – Sloped Differential Characteristic

The mechanism to send the blocking signal from the feeders to the main can take several different forms defending on the devices employed. The blocking signal can be sent by closing contact outputs on the feeders that energize a contact input on the main. The blocking signal could also be sent by a a messaging protocol such as IEC 61850 GOOSE messaging or other suitably fast messaging protocol.

The zone-selective-interlocking scheme must be coordinated so that the upstream breaker does not assert a trip with the non-coordinating element before the blocking signal is received from the downstream elements.

In order to coordinate the time delay on operation of the upstream, fast, non-coordinating element, the engineer must understand the operate time on the upstream device and the operate time on the downstream device. The time to operate the instantaneous overcurrent algorithm can vary based on the fault current, algorithm, and sample rate of the relay. Typical operate times of the algorithm can range from less than 4ms to less than 30ms. Added to the operate time will be the de-bounce time of the contact input on the upstream breaker and the contact closure on the downstream breaker. When engineering the zone interlocking scheme it is very important to understand how the relay's instantaneous overcurrent element will perform under fault conditions. Many relay manufactures will give operate times in the specification section of their manual. These operate times will be based on levels of pickup. Since the current phasor estimation is performed with a full-cycle Fourier filter, if the fault current level is very close to pick up, the element will take about one power system cycle to operate. The element should take less time to operate if the fault current level is greater than pickup. As an example of this phenomenon, the response time of a family of relay algorithms is shown in equation one below [2]:

$$t_{pkp} = \frac{1.33}{MOP} \quad \text{Equation 1}$$

In equation one, t_{pkp} is the time to pick up in cycles and MOP is the multiple of pickup. For a fault at exactly pickup, the element will take 1.33 cycles to operate. For a fault that is twice pick up the element will take 0.67 cycles to operate. Fig. 3 below illustrates this example by graphing operate time verses fault current for an element set with a pickup at 10KA.

In Fig. 3 the dashed bottom most line is the element operate time. The solid second line from the bottom is the time it takes for the relay to scan and assert logic. In a zone interlocking scheme, this line will define the time that the blocking signal must be received in. If the blocking signal is received after the inputs are scanned, the scheme will falsely operate for an out of zone fault. The third dashed line from the bottom is the operate time of the output contact and the top solid line is the time to clear the fault with a three cycle breaker.

Understanding of the algorithms is especially important if the relays employed use different algorithms. If a 10ms algorithm is used on the upstream breaker and a 30ms algorithm is used on the downstream breaker, the non-coordinating element on the upstream breaker must be time delayed by the 30ms operation time of the downstream breaker, the contact closure time of the downstream breaker and the de-bounce time of its own input. This could amount to a time delay 38 milliseconds.

Alternately, if the upstream and downstream relays use the same algorithm, and settings of debounce time of zero, a minimal or zero time delay can be employed.

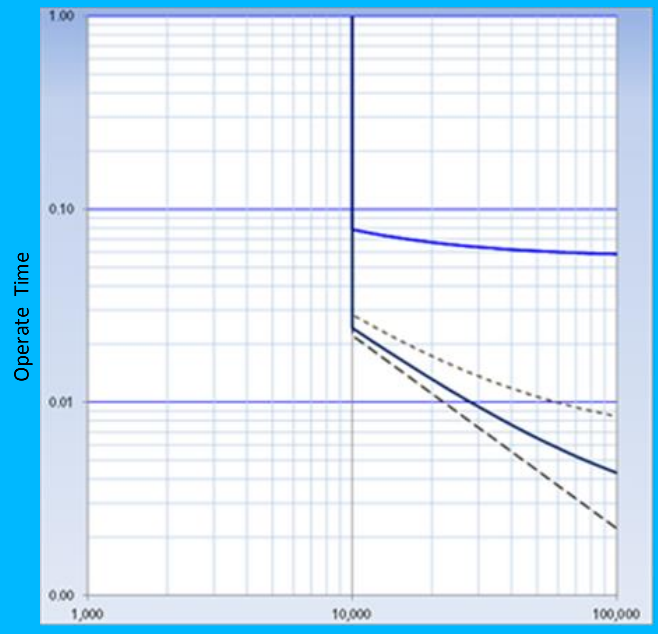

Fig. 3 – Operate Times for IOC

In order to examine the two systems, a dis-similar algorithm scheme and a similar algorithm scheme are examined.

In the dis-similar algorithm, assume a definite time overcurrent element on the upstream breaker with a time delay of 40ms and a contact operate of 4ms. If the fault current is 1.8 times pickup, equation 1 gives a time of 12ms to pick up. This pickup time and time delay would give a operate time of 56 milliseconds. With a three cycle breaker this would give a total clear time of 106milliseconds. This would give an arc flash incident energy level of over 7.5 for the 4KV system and over 12 for the 480V system. Twelve calories per centimeter squared is a threshold above which

PPE can become more cumbersome (**ref** NFPA 70E table) and since this solution exceeds that value, would not be very effective.

In a similar relay system, if the element is time delayed by 4ms, this would give an operate time of 16ms. With a three cycle breaker and a solid state output contact time of 0.1ms, this would give a total clear time of 66.7ms. This clearing time would result in incident energy of 5.8 calories per centimeter squared for the 480V system and 4.0 calories per centimeter squared for the 4KV system.

These two example solutions vary greatly in their incident energies and expose the need to understand the algorithms involved in the relay. Choosing the wrong algorithm can lead to insufficient mitigation of the incident energy and failure to understand the algorithm can cause the scheme to miss-operate.

IV. Case Study: Bus Differential Controlling Three-Cycle Circuit Breaker

A low impedance bus differential system will individually measure each breaker that is connected to the bus zone of protection. The vector sum of the primary values of these breaker currents will be the differential current. The largest of the breaker currents will be the restraint current. The bus differential element will operate when the differential current is greater than the pickup setting and greater than a percentage setting of the restraint current. The settings of pickup and slope on the restrained differential characteristics build a sloped differential characteristic and are shown in Fig. 3 below. In Fig. 3 the region above the curve is the operate region and the region below the curve is the restraint region. The sloped differential characteristic aids in overcoming unequal CT performance.

Fig. 3 – Sloped Differential Characteristic

Low impedance bus differential systems have an algorithm that can typically operate in less than one power system cycle. This would give an operation time of 16.7ms. With a solid state contact output, the contact could be asserted in 16.8ms from inception of the fault. With a three cycle breaker, this would give a total clear time of 66.7ms. If this clearing time is compared to the graphs in the appendix incident energy of 5.8cal/cm2 is calculated for the 480V system and incident energy of 4cal/cm2 results for the 4KV system. Neither of these incident energies is large enough to require cumbersome PPE.

The low impedance differential solution adds extra expense beyond the zone interlocking solution because it requires a dedicated device for bus differential. Since this is low impedance differential scheme, the current transformers can be wired “through” the breaker relays, so no additional current transformers are necessary for this solution. The low impedance solution requires no signaling between the relays and no coordination of algorithms so it is simpler than the zone interlocking scheme in a typical medium voltage application. Additionally, the low impedance differential will operate for a bolted fault which wouldn’t produce light, so it is more dependable than the arc-flash schemes.

The arc-flash relay does offer faster clearing times than the zone-selective-interlocking or the bus differential solution. In this model system, however; the extra benefit is small since both solutions allow the same type of clothing to be donned. The bus differential solutions gives additional benefit in that it will operate fast for bolted faults that won’t produce enough light to operate an arc-flash relay. With an arc-flash relay as the primary mitigation device, a bolted fault would have to be cleared by traditional overcurrent protection. For this reason bus differential and zone interlocking may be considered to provide better equipment protection.

V. Case Study: Reduced Energy Let Through Switch

A reduced energy let-through-switch, also known as a maintenance switch, or arc flash switch, is a switch which enables a non-coordinating element on the upstream device which can quickly clear the fault. The switch will have a maintenance mode and a normal mode. In the normal mode the non-coordinating element is blocked from operation and coordinating time overcurrents would be required to clear the fault. In the maintenance mode, the non-coordinating element is allowed to trip the upstream breaker “fast” without coordination with the downstream overcurrent elements. This switch is meant to be placed into “maintenance mode” when personnel are within the arc-flash boundary. Since the switch is used for personnel protection, it must have a means of positively identifying that the enhanced protection is in effect. Also, since the switch will enable non-coordinating elements, it should have a means of identifying when those elements are enabled so that the switch can correctly be placed into “normal” mode when work is completed. The identification of the switch position is usually indicated with lights from auxiliary switch inputs and alarms to a digital control system (DCS).

Operate time of the reduced energy element will be the same operate time as the instantaneous overcurrent element discussed with the zone interlocking scheme. The zone interlocking scheme will achieve similar incident energies as the bus differential scheme, as long as no additional delays are added to the upstream IOC element to accommodate extra time required to process the blocking signal.

The major drawback to the RELT scheme is that it requires the operations personnel to take action to enhance protection. This is considered an administrative procedure in ANSI safety standards. It is a low ranking hazard mitigation solution because, if personnel forget to enable the RELT switch prior to starting work, they will be exposed to much higher incident energies.

VI. Case Study: Impact of Five-Cycle Circuit Breaker Instead of a Three-Cycle Circuit Breaker.

In each of the cases discussed so far a three cycle breaker has been assumed. The possibility exists that a five cycle breaker could be used rather than a three cycle breaker. Table 1 below shows how a five cycle breaker would affect the incident energies verses a three cycle breaker.

Solution	IE with 3 cycle breaker in Cal/Cm2	Clearing Time in milliseconds	IE with 5 cycle breaker in Cal/Cm2	Clearing Time in milliseconds
480V 4ms Arc-Flash Sensor @ 25KA	4.8	54.1	7.5	87.4
480V 8ms Arc-Flash Sensor @ 25KA	5.0	58.1	8.0	91.4
4KV 4ms Arc-Flash Sensor @25KA	3.4	54.1	5.3	87.4
4KV 8ms Arc-Flash Sensor @25KA	3.5	58.1	5.4	91.4
480V Zone Interlocking 56ms sc@25KA	12.0	106.0	OVER 12	139.3
4KV Zone Interlocking 56ms sc@25KA	7.5	106.0	OVER 12	139.3
480V Zone Interlocking 56ms sc@25KA	5.8	66.7	8.7	100.0
4KV Zone Interlocking 56ms sc@25KA	4.0	66.7	6.0	100.0
480V Low Imp Bus Diff @25KA	5.8	66.7	8.7	100.0
4KV Low Imp Buss Diff @25KA	4.0	66.7	6.0	100.0

TABLE 1 – Incident Energies for Each Solution.

As seen in Table 1 the speed of the breaker affects the incident energy more than the mitigation technic. Any arc-flash mitigation program should also consider at the circuit breakers installed and consideration should be given to replacing five cycle breaker with faster three cycle circuit breakers.

VII. Conclusions

Light sensing relays that sense an arc flash event via light have the fastest operating times of any of the solutions discussed. As seen in Table 1, the benefit of arc-flash relaying is minimal in these test cases, since all of the mitigation techniques discussed moved the incident energy below a threshold of 12cal/cm^2 associated with more cumbersome PPE. Additionally, the arc-flash relay may introduce difficulties in testing the device in the field compared to traditional schemes like bus differential or zone interlocking. The arc-flash relay also has limitations on the type of faults it can detect. A bolted three phase fault will not produce an arc so the arc flash relay would not operate for that type of fault. This would allow the fault to persist much longer, and cause more equipment damage compared to a zone interlocking scheme or bus differential scheme.

A zone-selective-interlocking scheme adds some complexity due to the fact that the fast algorithms must be available in the relay specified and the designer must understand the operation of the algorithms involved to coordinate the time delay of the upstream device.

Testing can be challenging with each scheme. Zone-selective-interlocking can impose challenges to testers verifying that the scheme works as expected since they will have to test that the blocking signal is actuated from the downstream device current and is received and processed properly by the upstream device. Arc Flash relays must be tested with their actuating quantities which will include a combination of light, current, and/or pressure. Most relay test sets can provide multiple sets of currents so low impedance bus differential protection can easily be tested, but the relay must be "phased" once load is picked up to insure that no current transformer circuits are wired incorrectly. If the bus differential circuit isn't properly wired and commissioned, it can cause miss-operations when load is fed from the bus.

Biographies

Terrence Smith is the lead P&C Technical Application Engineer for GE Grid Solutions North American Commercial team. He has been with GE since 2008 supporting the Grid Solutions Protection and Control Portfolio. Prior to joining GE, Terrence has been with the Tennessee Valley Authority as a Principal Engineer and MESA Associates as Program Manager. He received his Bachelor of Science in Engineering majoring in Electrical Engineering from the University of Tennessee at Chattanooga in 1993 and is a professional Engineer registered in the state of Tennessee.

Christopher Burnette received his B.S. and M.S. degrees in Electrical Engineering from Clemson University in Clemson, SC. He joined the GE Industrial Solutions Division in 2007 and currently holds the position of Lead Power Systems Engineer for the Georgia/Florida/Caribbean District based in Atlanta, Georgia. Mr. Burnette is a Registered Professional Engineer in the states of Tennessee, Georgia and Florida.

Marcelo E. Valdes graduated from Cornell University in 1977 with a BS in electrical engineering. Currently he is Global Applications Leader, Product Management Components for GE Industrial Solutions. He has been with GE over 38 years, in field engineering, sales, marketing, and application engineering. Mr. Valdes is past chair of the IEEE Power and Industrial Applications Engineering chapter in San Jose, CA, and the Industrial Applications chapter in San Francisco, CA. Mr. Valdes has authored and co-authored over 30 papers for IEEE and other engineering forums, and holds 20 patents in the field of power systems protection and circuit breaker trip systems. Mr. Valdes chaired IEEE 1683, Guide for Safe Low Voltage Motor Control Centers published in August 2014, and a member of several other IEEE standard working groups and an IEEE IAS distinguished lecturer for 2014/15 and was the chair of the IEEE Electrical Safety Workshop in 2014.

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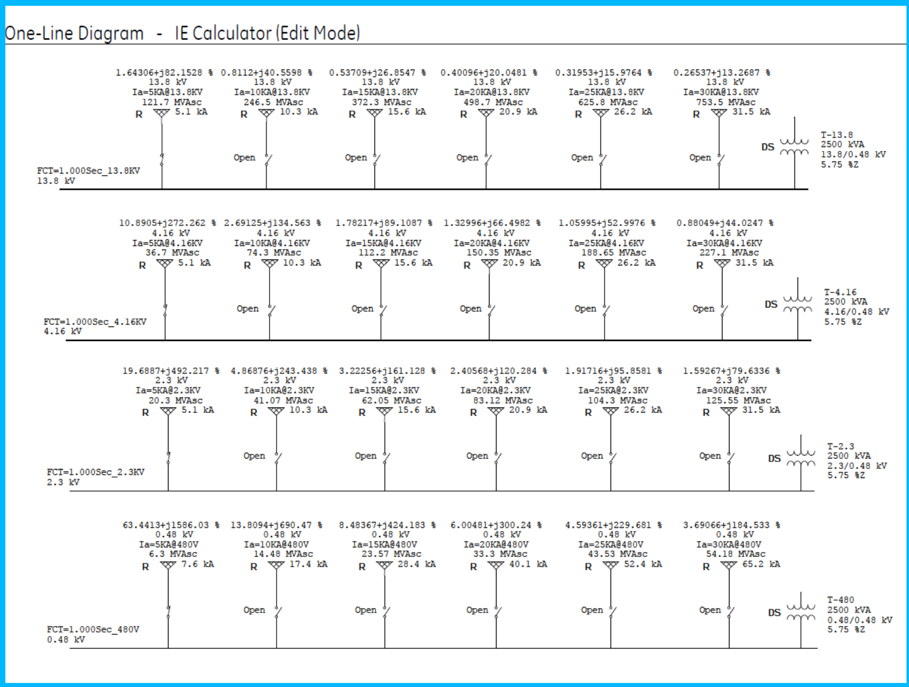
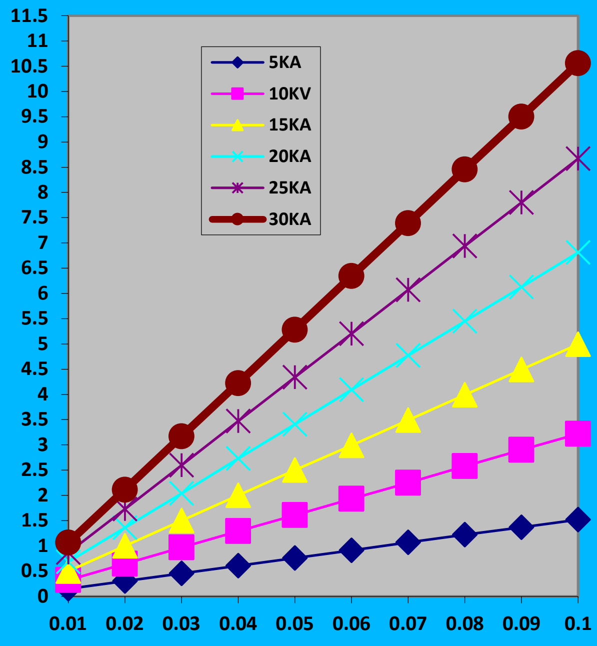
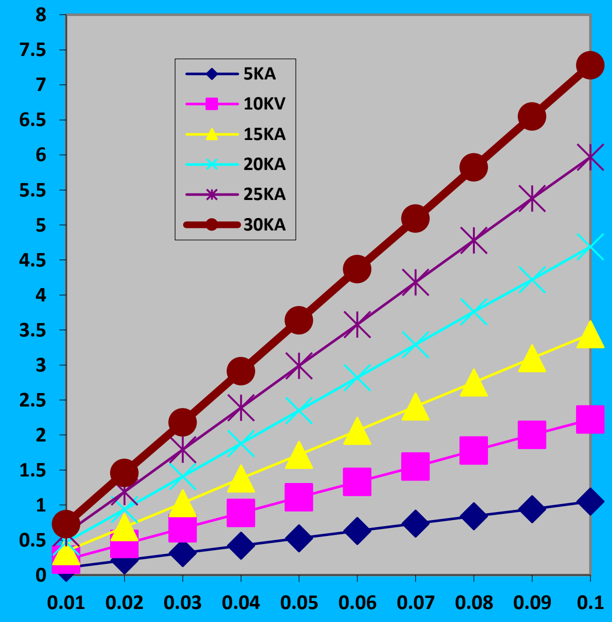
Appendix A – Model System



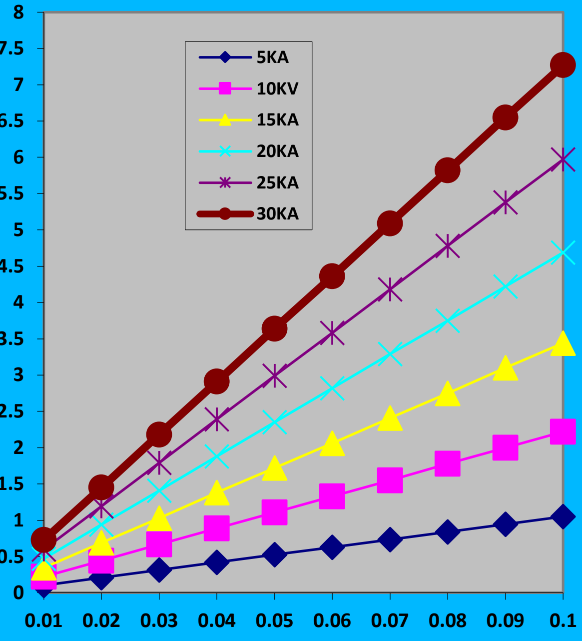
Appendix B – Incident Energy verses clearing time graphs



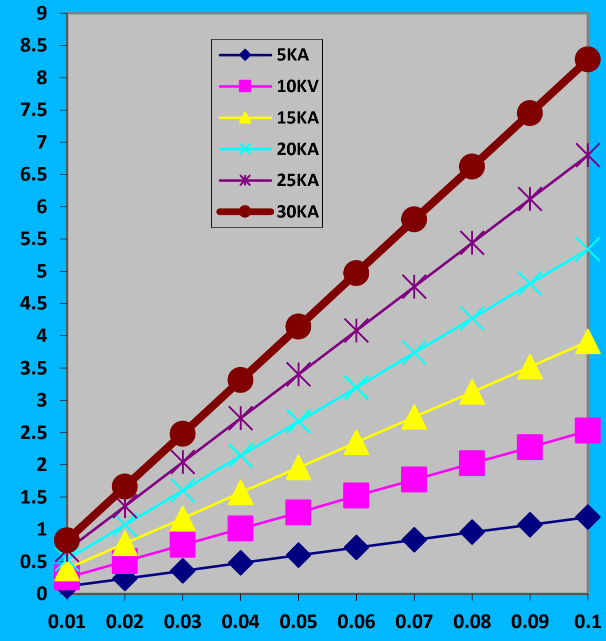
480V Clearing Times Verses Incident Energy



4KV Clearing Times Verses Incident Energy



2.3KV Clearing Times Verses Incident Energy



13.8KV Clearing Times Verses Incident Energy