Bus Protection
A New and Reliable Approach

Vincent Duong, P.E., PMP
Dist. Protection and Automation, ABB Inc.
Coral Springs, USA
vincent.duong@us.abb.com

Jay Cueco, P.E.
Technical Services Equipment, NextEra Energy
Juno Beach, USA
Jay.Cueco@nexteraenergy.com

***Abstract*--This paper presents a new and reliable method of bus protection scheme that can be applied to either radially fed or multi-incoming source bus works. The scheme will reliably protect the bus against internal faults and will securely trip the appropriate breaker for external (through) faults. It is immune to the weakness of CT saturation present in conventional differential schemes and will have acceptable operating speed. It is designed with a fail-safe mode that removes the need for a physical relay redundancy. The fail-safe mode automatically evokes the equivalent backup logic once the primary relay failure is detected; hence a lengthy bus outage can be avoided. The scheme is suitable to be applied on switchgear and substation bus works.**

The paper also addresses several benefits with the implementation of IEC61850 Standard to this new bus protection scheme; including protection reliability and security, relay interoperability, ease of system expansion, and cost savings.

I. Introduction

Substation or switchgear bus is one of the most critical elements because it is the conjunction point of electric power flow. Bus protection against electrical faults are required in order to avoid life threatening event, severe equipment damage, or interrupted electric service. There are myriad methods of bus protection, such as high impedance bus differential, low impedance bus differential, switchgear arc flash protection, etc.. Each one can adequately serve its own designed purpose but adversely has its own limitations. This paper introduces a new bus protection scheme utilizing IEC61850 GOOSE communication that is immune to most known limitations but very reliable and within acceptable operating speed.

II. Why Bus Protection

Due to the critical nature of the bus component in the power system, a reliable method must be implemented to prevent bus faults from damaging equipment and disrupting system stability. An internal bus fault without proper relay protection may cause rapid severe damage due to the high magnitude of currents involved and typically develop into a sustained loss of high value power system components. Conventional Bus Protection schemes such as the High Impedance Differential, Low Impedance Differential and Arc Flash Detection have been adopted in the industry to provide protection with a focus on high speed and secure operation. However, the commonly adopted bus protection schemes have disadvantages varying from the possible mis-operation due to CT saturation in High/Low Impedance Differential schemes, equipment inflexibility when adding new sources/loads in High/Low Impedance Differential schemes, and potential insensitivity for low impedance faults in Arc Flash detection. The new approach described in this paper attempts to provide comparable bus protection without the disadvantages inherent in the conventional schemes that are widely adopted in the industry.

III. Bus Protection Methods

Low impedance differential and high impedance differential methods are typically utilized for substation and switchgear buses including single bus, transfer bus and breaker-and-a-half bus arrangements. While arc flash detection method is applied for enclosed switchgear bus only.

A. Low Impedance Differential

The Low Impedance Differential scheme applies Kirchoff's Current Law where the summation of CT

secondary currents flowing into the junction point is monitored by an overcurrent relay.

Ideally the summation of the CT secondary currents would be zero during normal conditions or during an external fault event. An internal bus fault will cause a proportionate CT secondary current to flow into the junction point which will cause the overcurrent relay to operate.

Since the possibility of CT saturation can occur on faulted circuit during an external fault event, the overcurrent relay pickup setting must be de-sensitized appropriately to maintain correct operation. Additionally, a time-delay element may be required in order to suppress tripping during severe CT saturation in one of the circuit elements.

In order to maintain proper operation due to CT saturation, a thorough engineering assessment for CT performance must be completed in order to calculate the proper pickup setting and time delays. Compared to the other conventional schemes, the Low Impedance Differential method is typically less sensitive and may potentially be slower to operate due to the addition of time delays.

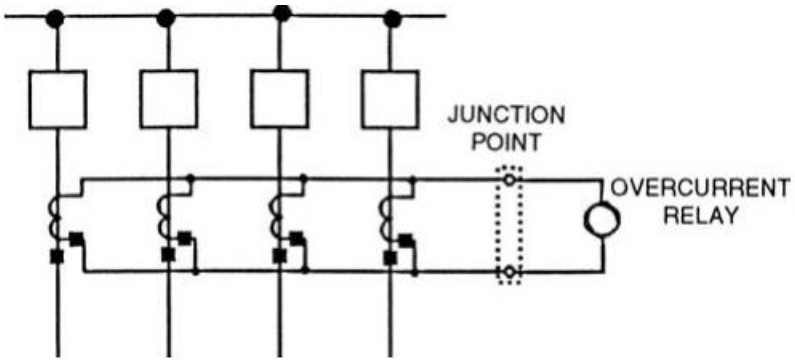

Figure 1: Low Impedance Differential Single Line Diagram

B. High Impedance Differential

The High Impedance Differential scheme also applies the concept of Kirchoff's Current Law as with the Low Impedance scheme but with the addition of a high impedance relay. This scheme overcomes potential CT response dissimilarities by imposing the CT secondary currents through the high impedance component and thus creating a voltage across the impedance which is monitored by the relay.

Ideally, the current magnitude through the high impedance component will be close to zero during an external fault event or during normal system conditions. During an internal bus fault, high current magnitudes will be imposed through the high impedance component causing a large voltage across which will be detected by the relay in order to initiate high speed operation. Due to potentially large voltages across the high impedance component during internal bus faults, additional circuit components such a varistor may be necessary to maintain safe operation.

Although the High Impedance Differential scheme offers sensitivity and high speed operation compared to the Low Impedance method; the scheme must be properly designed through a rigorous engineering study which must take into account proper CT selection, burden calculations and overall wiring design to the junction point. The general disadvantages of this scheme include inflexibility of CT selection, possible difficulties when adding new loads/sources and the potentially time-consuming engineering design efforts necessary for reliable operation.

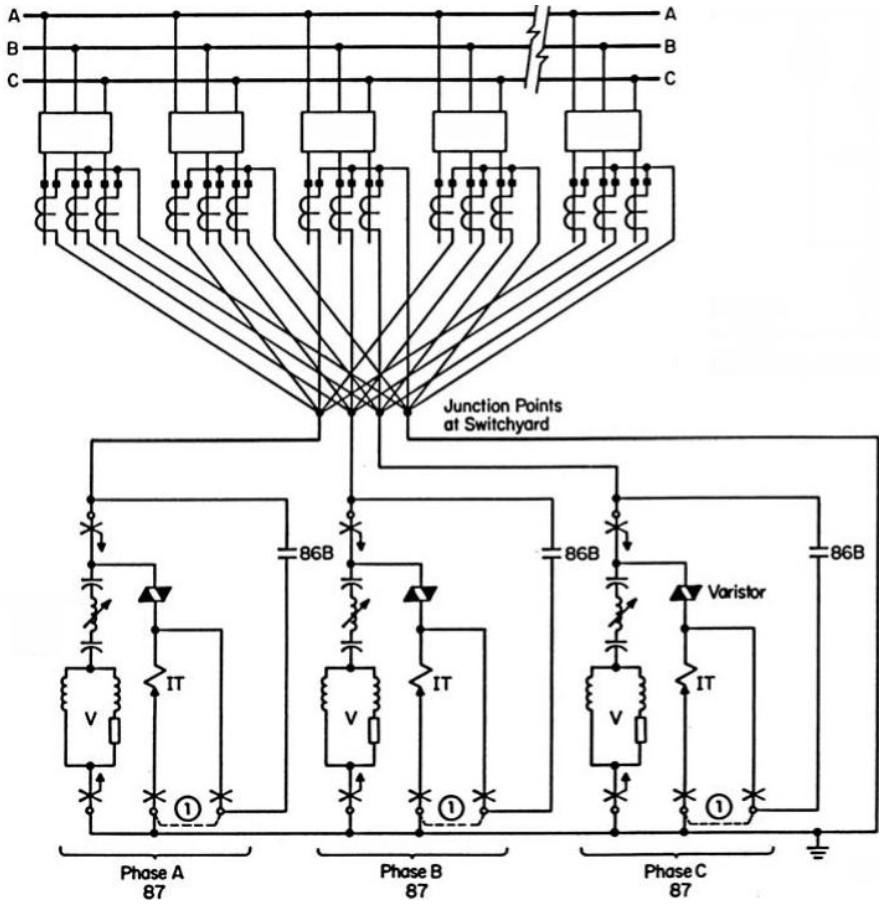

Figure 2: High Impedance Bus Differential Circuit

C. Arc Flash Detection

The Arc Flash Detection scheme is typically used to protect bus components within an enclosed switchgear lineup. In this scheme, microprocessor relays are used in combination with fiber loops or fiber point sensors located strategically throughout the switchgear to detect the light discharge caused by an arc hazard event.

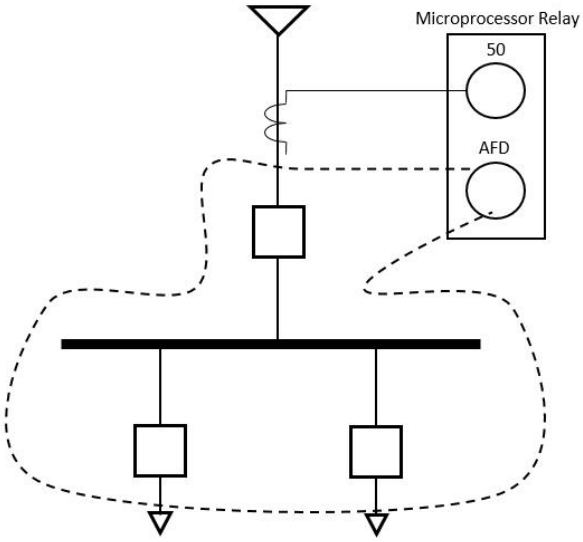

Figure 3: Arc Flash Detection Single Line Diagram

Ideally, the light sensitive fiber components are deployed throughout the switchgear bays to fully encompass all areas where an arc flash event may occur. In addition to the light sensor, the Arc Flash microprocessor relay may also enable an overcurrent element as part of the logic tripping decision in order to prevent false tripping operations. During an external fault, the fiber components should not sense any abnormal light levels. For an internal bus fault with sufficient impedance to cause an arc flash, the fiber components should be able to detect abnormal light levels and initiate high speed operation. In order to maintain proper operation, the Arc Flash microprocessor relays must be carefully calibrated to operate only for abnormal light levels.

Although the Arc Flash Detection scheme offers high speed operation, the general disadvantages of the scheme include, potential insensitivity to low impedance bus faults, the proper management of sensitive fiber components and its inapplicability towards configurations other than enclosed switchgear.

IV. Introducing the "Novel" Bus Protection Scheme

Besides the limitations of the bus protection methods described above, the common problem is they are not easy to be modified as system parameters change; whether it is a system expansion or an increase in available system fault current. In addition there is no effective way for a single bus protection relay to be applied to the buses configured in "double-bus single-breaker" arrangement shown below in Figure 4.

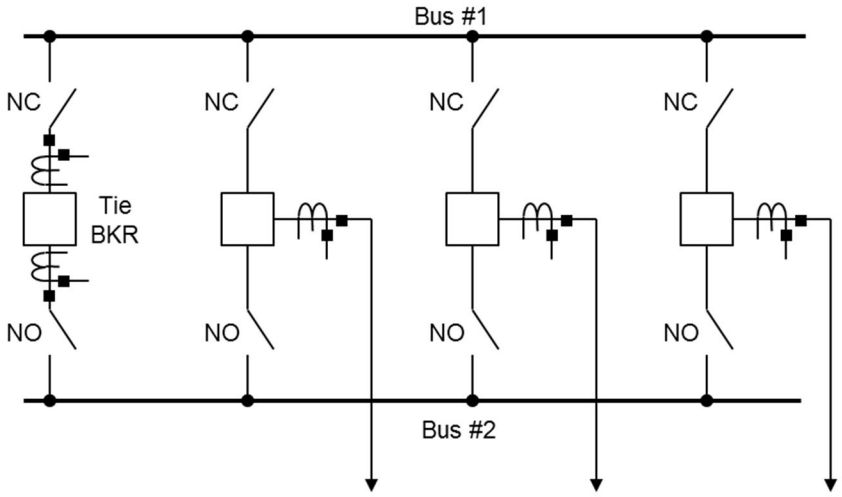

Figure 4: Double Bus Single Breaker Arrangement

Despite there are several arrangements in substation or switchgear, a bus is an electrical element represented by a convergence of incoming (source) and outgoing (feeder) points. Each incoming/outgoing point has an associated circuit breaker for fast interruption purpose if a fault is detected in the bus. A simplified single line diagram is shown in Figure 5 below and will be used as discussion and illustration purposes throughout this paper.

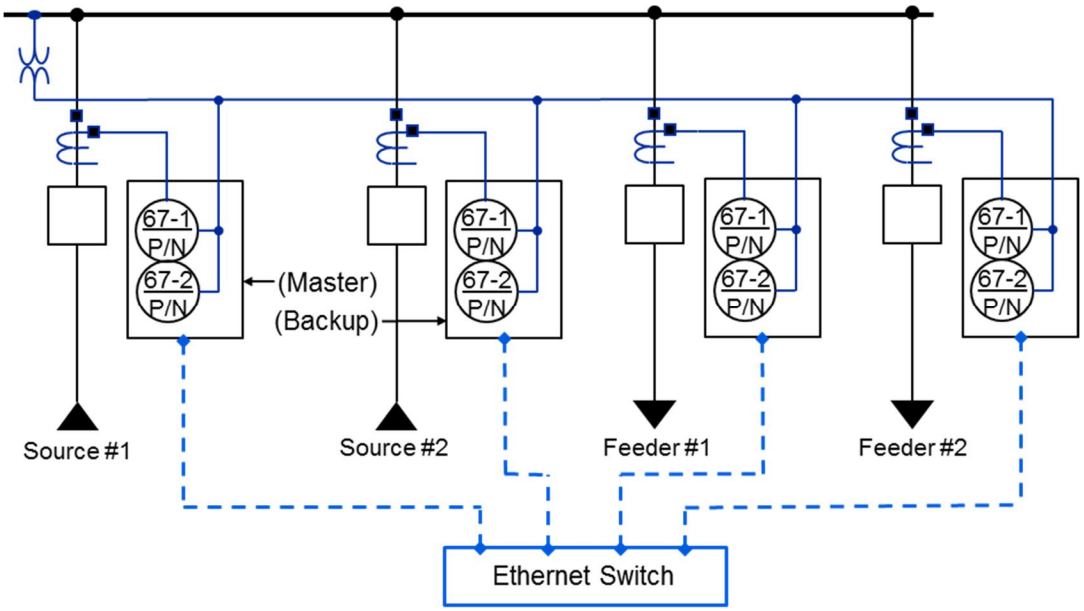

Figure 5: Diagram of "Novel" Bus Protection Scheme

Unique features of this approach of bus protection scheme include:

- There are multiple incoming/contributing sources
- A dedicated bus protection relay is not required
- The bus protection is accomplished by each breaker's associated relay, which is usually already existing, i.e. feeder protection relay and breaker failure relay
- A "master" relay is assigned to perform the bus protection scheme
- A "backup" relay automatically assumes the bus protection scheme if the "master" relay failure occurs
- All contributing relays are communicating to the "master" and "backup" relays via Ethernet based IEC61850 GOOSE communication

V. Scheme Development

The relays shown in Figured 5 for bus protection scheme shall have these required functions and features:

- IEC61850 compliant and capable of GOOSE communication
  - If the constant integrity/quality check of the GOOSE communication is bad, the scheme shall be disabled and an alarm is issued immediately
- Two phase and ground directional overcurrent elements:
  - 67P/N-1 as reverse direction (REV) for detecting fault current flow into the bus
  - 67P/N-2 as forward direction (FWD) for both detecting and tripping fault current flow out of the bus (through fault)

The principle of operation is to have all contributing circuit breakers tripped when at least one reverse direction (REV) element is detected and not any forward direction (FWD) element is pending (Figure 6).

Should there be a through fault, i.e. a feeder fault, the individual FWD of the associated relay must operate to trip its own circuit breaker only (Figure 7).

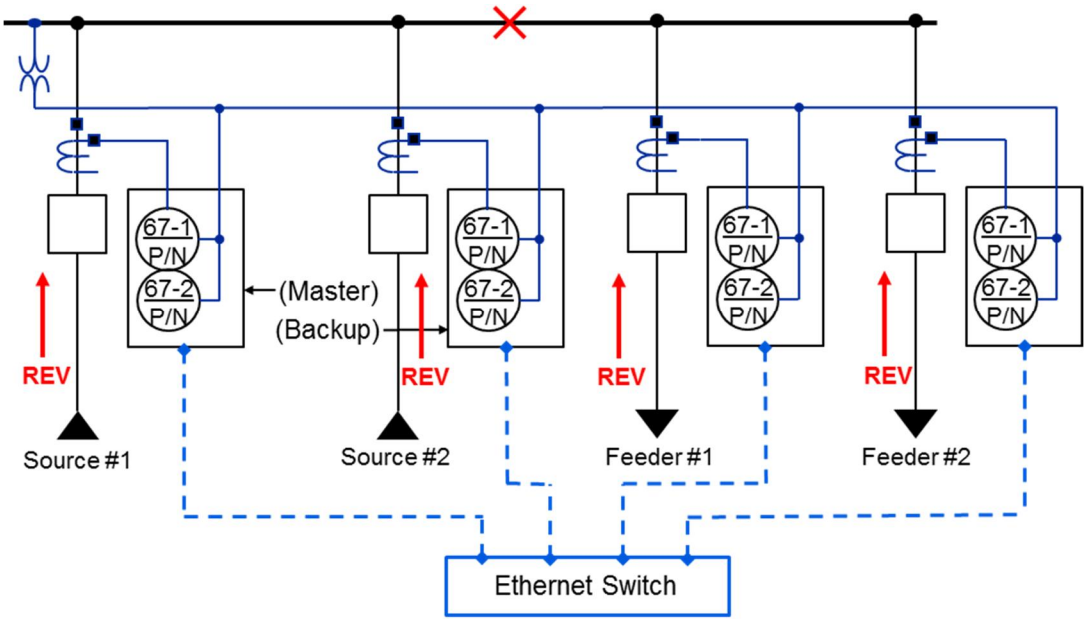

Figure 6: Bus Fault – No FWD Element Detected by any Individual Relay

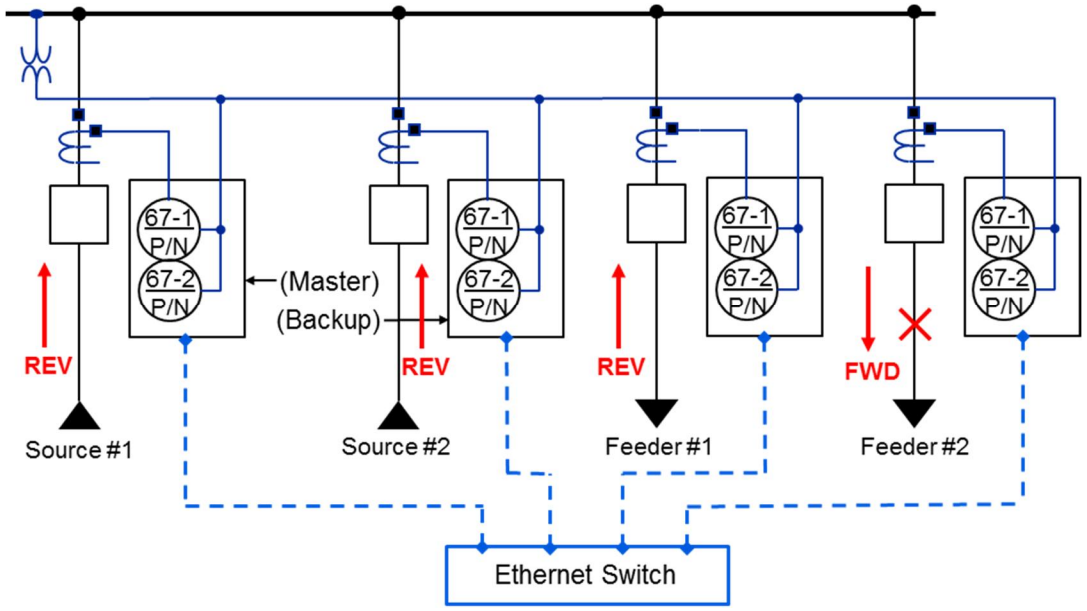

Figure 7: Feeder #2 Fault (Through Fault)

The "Master" relay is to process operation information from itself as well as all contributing "Peer" relays via GOOSE communication. The logic has to be sensitive and fast enough to trip for bus fault and has to be secured to not trip for feeder fault or through fault. The logic diagram for bus fault shown in Figure 8 consists of the following important factors:

- GOOSE_VALID is used to arm the bus protection scheme; if GOOSE integrity check fails, the scheme is disabled and an alarm is raised immediately.
- When a fault is on a feeder and outside the bus zone (through fault condition), the impacted feeder relay will trip on its own FWD element. The bus protection scheme will not operate even though the rest of the relays detect REV element

at the same time. Even CT saturation on the impacted feeder is likely, its relay still trips by FWD element and will not affect the bus protection scheme operation.

- When a fault is on the protected bus, each contributing relay will NOT detect any FWD and will have one or more REV elements operated. Hence the TRIP_BUS output will trip and block close all contributing circuit breakers.
- Circuit breaker open condition is incorporated in the scheme. When the scheme operates for a bus fault, the TRIP_BUS output signal is held high by an SR (flip-flop) logic gate and will be reset after all contributing breakers are confirmed open. In case when a breaker is already open for some reason, the associated relay will not report FWD and REV signal under bus fault condition and will not affect the bus protection scheme operation.
- The scheme can be easily accommodating additional sources/feeders – a real flexibility for system expansion.

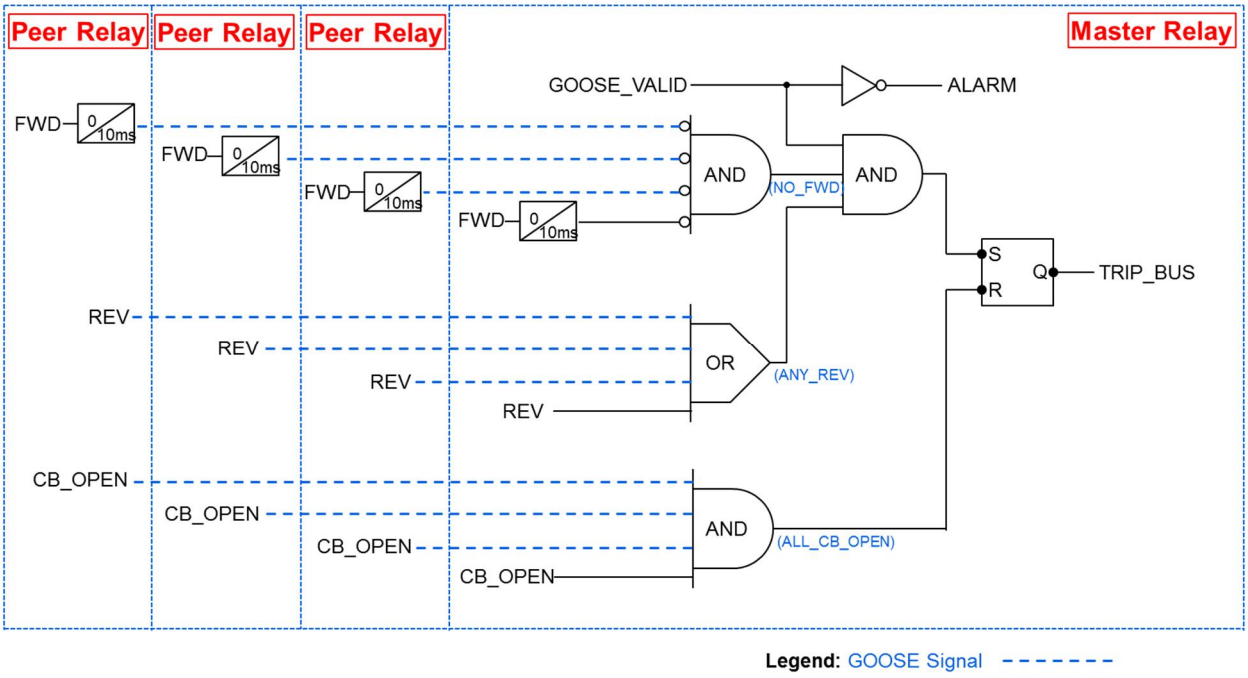

Figure 8: Logic Diagram - Bus Protection Scheme

VI. Scheme Validation and Testing

The scheme must be validated in order to ensure the desired results and to record the scheme operation speeds. Setups include four ABB micro-processing multi-functional type REF615 feeder protection relays with four breaker simulators, one 16-port industrial grade RUGGEDCOM managed Ethernet switch, and one Omicron test set.

67P/N-1 (REV) and 67P/N-2 (FWD) elements are set to trip minimum fault current, 0° (zero degree) characteristic angle, ANSI Definite Time curve with 40ms trip delay time, and instantaneous reset. Note the 40ms trip delay time is the relay's inherent operating time for the directional elements to confirm polarization from bus voltage. Four currents are simultaneously injected by the test set, with 0° phase angle as forward direction and 180° phase angle as reverse direction. To simulate a bus fault, all four currents are in reverse direction; for a feeder fault (through fault), the impacted feeder current is in forward direction and the other three in reverse direction. When a relay trip its own breaker, the associated current injection will be stopped to mimic the fault current having been interrupted and the remaining (un-faulted) circuits will resume to their normal conditions.

Each bus fault and through fault scenario was undergone at least ten (10) trials. Test results under bus fault condition were all correct. However the results

under through fault condition were inconsistent – in several tries all breaker tripped as if it was a bus fault. The reason was related to the instantaneous reset of both 67P/N-1 (REV) and 67P/N-2 (FWD) elements, which raced to reset themselves once the fault current injection had stopped. For example a through fault was simulated on Feeder #2, if its FWD element reset slightly ahead of the other REV elements, the scheme would mis-operate. Therefore a drop-out time of 10ms was added to the FWD elements (Figure 8); and the through fault test results were all correct.

The "processing" times for bus fault (per Figure 6) and through fault (per Figure 7) are summarized in Tables 1 and 2 below. The processing times are recorded by the Omicron test set which include relay fault intercept time, 67P/N operating time (40ms), and GOOSE traffic time (typically 4ms).

Trials	Processing Time (ms)	Processing Time (cy)
1	50.50	3.03
2	51.00	3.06
3	49.70	2.98
4	55.30	3.32
5	51.50	3.09
6	51.80	3.11
7	52.10	3.13
8	55.20	3.31
9	56.60	3.40
10	54.20	3.25
Average	**52.79**	**3.17**

Table 1: Scheme Operating Time for Bus Fault

Trials	Processing Time (ms)	Processing Time (cy)
1	50.10	3.01
2	53.20	3.19
3	53.20	3.19
4	50.90	3.05
5	51.20	3.07
6	51.60	3.10
7	56.10	3.37
8	51.20	3.07
9	53.30	3.20
10	55.50	3.33
Average	**52.63**	**3.16**

Table 2: Scheme Operating Time for Through Fault

VII. Redundancy in Protection

A special characteristic about the scheme is to have a "master" relay processed the core function of the bus protection. However the scheme will cease to provide bus protection if the master fails for any reason. To cope with this situation, a "backup" relay with the same scheme shown in Figure 8 is programmed to assume the bus protection once the master relay failure signal is received. This is done by wiring the IRF output from the master relay to the backup relay that provokes the same programmed logic for bus protection scheme. Then the backup relay will open (transfer trip) the master relay's associated breaker through hard wire since the master relay failure is confirmed (Figure 9). With master relay's

circuit breaker open status, the bus protection scheme should not have any concern of mis-operation since there is no possible fault current path/contribution (from the isolated source) to the system.

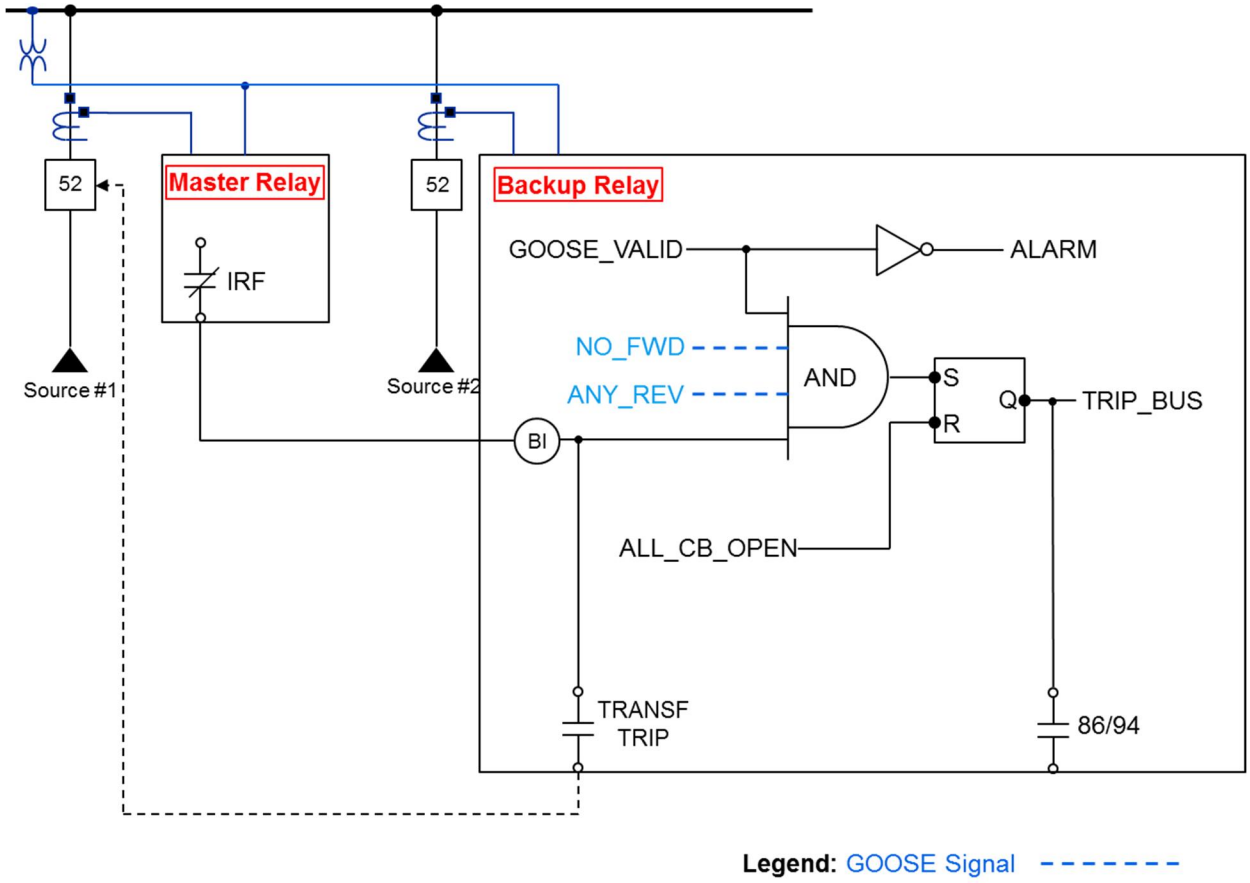

Figure 9: Bus Protection Redundant Logic in the Backup Relay

VIII. Consideration in Communication Network Topology

Utilization of IEC61850 GOOSE communication for the scheme will greatly reduce cross wiring among the contributing relays; hence it directly means huge savings in engineering, installation labor/time, and materials associated to the traditional copper wiring approach. However the bus protection scheme will be disabled if GOOSE communication interruption is detected, i.e. broken Ethernet cable or failed Ethernet switch. GOOSE_VALID alarm is issued following a GOOSE communication interruption for the purpose of immediate action by the operator; therefore the system is relatively safe because, by probability, a bus or through fault would not occur simultaneously.

Advanced IEC61850 compliant micro-processor relays are usually equipped with multiple Ethernet ports that are capable with Parallel Redundancy Protocol (PRP) according to IEC62439. In order to eliminate the possibility of GOOSE interruption and to achieve 100% communication availability, one can consider the implementation of double-star (Figure 10) or self-healing ring (Figure 11) network topology.

Either communication network topology works fine; however the double-star is preferred because of the following characteristics: less disturbance to the network with future expansion (for adding connected relays), faster trouble shooting, minimum communication latency, and ease of maintenance.

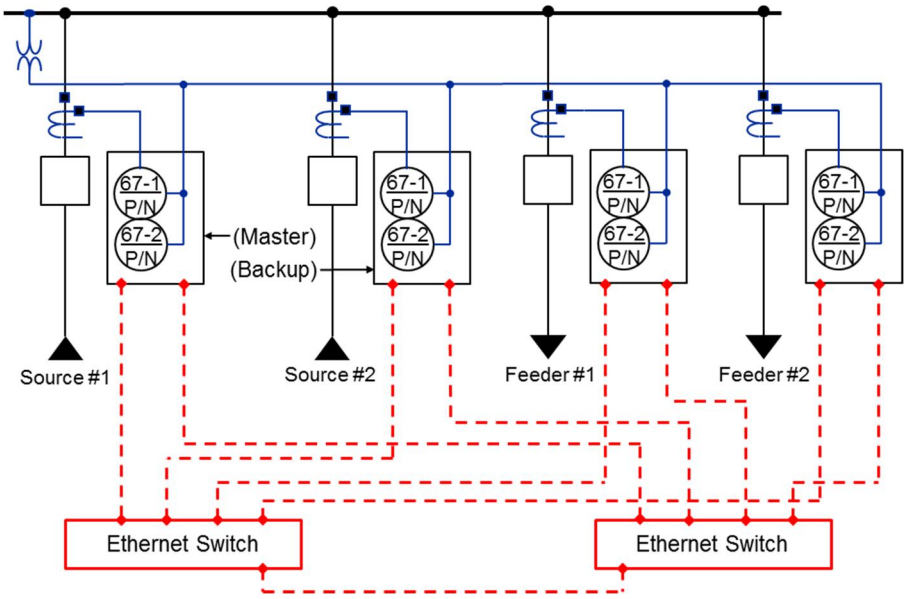

Figure 10: Double-Star Communication Network Topology

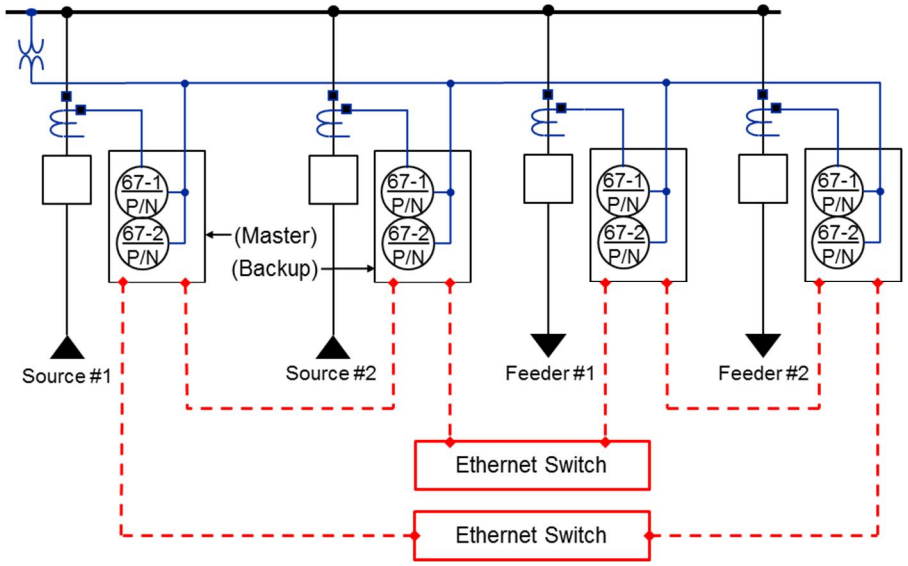

Figure 11: Self-Healing Ring Communication Network Topology

IX. Summary

This scheme can provide a good bus protection by utilizing the existing contributing circuit breakers' associated feeder relays. It is never an intention for the scheme to replace an already installed bus protection relay. It is rather a no-cost parallel bus protection in addition to an existing high impedance or low impedance differential relay. Nevertheless it is an ideal solution to existing systems in need of bus protection with any of these conditions:

- Double-bus single-breaker bus arrangement (Figure 4)
- Circuit breaker lacking a dedicated CT for differential relay
- Existing switchgear lacking cubicle/panel space for a stand-alone differential relay
- Difficulty for additional wiring associated to a stand-alone differential relay
- Cost consideration to modify the existing system for an added differential relay

- A supplement to switchgear arc fault relay (Figure 3)

X. Conclusion

The scheme is proven to operate correctly and securely against bus fault and through fault conditions with acceptable operating speed, even under CT saturation. It can be applied to any bus configuration including the double-bus single-breaker arrangement – as a stand-alone or a supplement bus protection scheme. The core logic of the scheme is simple yet effective for protecting substation and switchgear buses with one or multiple contributing sources. The core logic can easily be modified to adapt changes in electric system or in adding/subtracting contributing circuit breakers.

Operating speed largely depends on the operating time of directional overcurrent elements (67P/N-1 and 67P/N-2). If the 67 element speed is improved to be 20ms, then the scheme total operating time is reduced to less than 33ms (≈ 53ms – 20ms, see Tables 1 and 2). Micro-processor relays capable of IEC61850 GOOSE communication and Parallel Redundancy Protocol in double-star or self-healing ring network topology (Figures 10 and 11) will achieve 100% communication network availability. The automatic backup protection scheme illustrated in Figure 9 is a no-cost and effective approach that enhances the reliability of the scheme.

REFERENCES

[1] Walter A. Elmore (2004). *Protective Relaying Theory and Applications*, Second Edition, Revised and Expanded. ISBN 0-8247-0972-1, ABB Power T&D Company Inc.

[2] Suhag P. Patel. *Affordable Bus Protection Schemes for Radial Distribution Substations*.

[3] IEC61850-8-1 (2011), *Communication Networks and Systems in Substations – Part 8-1*.

[4] Hubert Kirrmann, Peter Reitmann and Steven Kunsman (2008), *Network Redundancy Using IEC62439*, PAC World.

BIOGRAPHICAL SKETCHES

Vincent G. Duong, P.E., PMP currently holds an Account Development Manager position in Distribution Protection and Automation group at ABB. He received his BSEE degree with Power System Specialization from the University of Alberta in Edmonton, Canada; and both MBA and MS in Operations and Project Management degrees from Southern New Hampshire University in Manchester, New Hampshire. Vincent has spent most of his career in distribution and transmission protection and controls engineering, including system modeling, study, design, relay settings, and system disturbance analysis. He is also actively involved in customer training and power system protection-coordination instruction. He is an IEEE member, a registered Professional Engineer of New Hampshire, and Project Management Professional of Project Management Institute (PMI).

Jay Cueco, P.E. was a Senior Application Engineer position in Distribution Protection and Automation group at ABB. He is currently a Sr. Engineer at NextEra Energy. He received his BSEE degree with Power System Specialization from the Florida International University, Miami, Florida. Jay has spent most of his career in distribution and generation protection and controls engineering, including system/plant modeling, study, design, relay settings calculation, and fault analysis. In his current role, Jay is responsible for customer training, application scope analysis and development of protection and control schemes. He is an IEEE member, a registered Professional Engineer of Ohio.