High-Impedance Bus Differential Misoperation Due to Circuit Breaker Restrikes

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Introduction

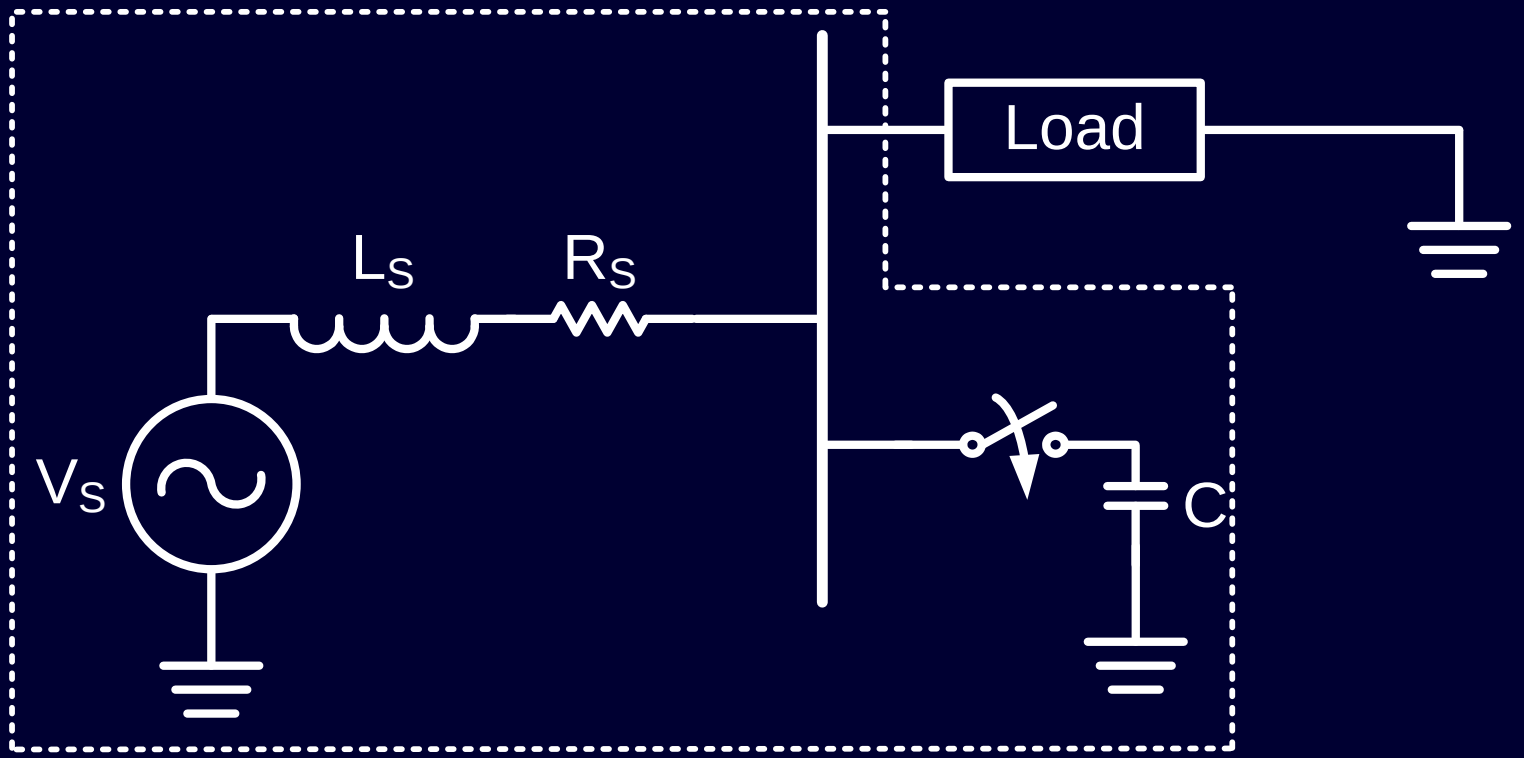
- Shunt capacitor banks
- Capacitive switching transients
- Surge arresters
- High-impedance bus differential protection
- Real-world event analysis showing relay misoperation due to circuit breaker restrike

Shunt Capacitor Banks

- Installed at all voltage levels
- Support voltage and reactive power (VAR)

Capacitive Switching

Causes transient-related issues, which increase with voltage level and X/R ratio



Capacitor Inrush

Inrush current

$$i(t) = \frac{V(0)}{Z_0} \sin(\omega_0 t)$$

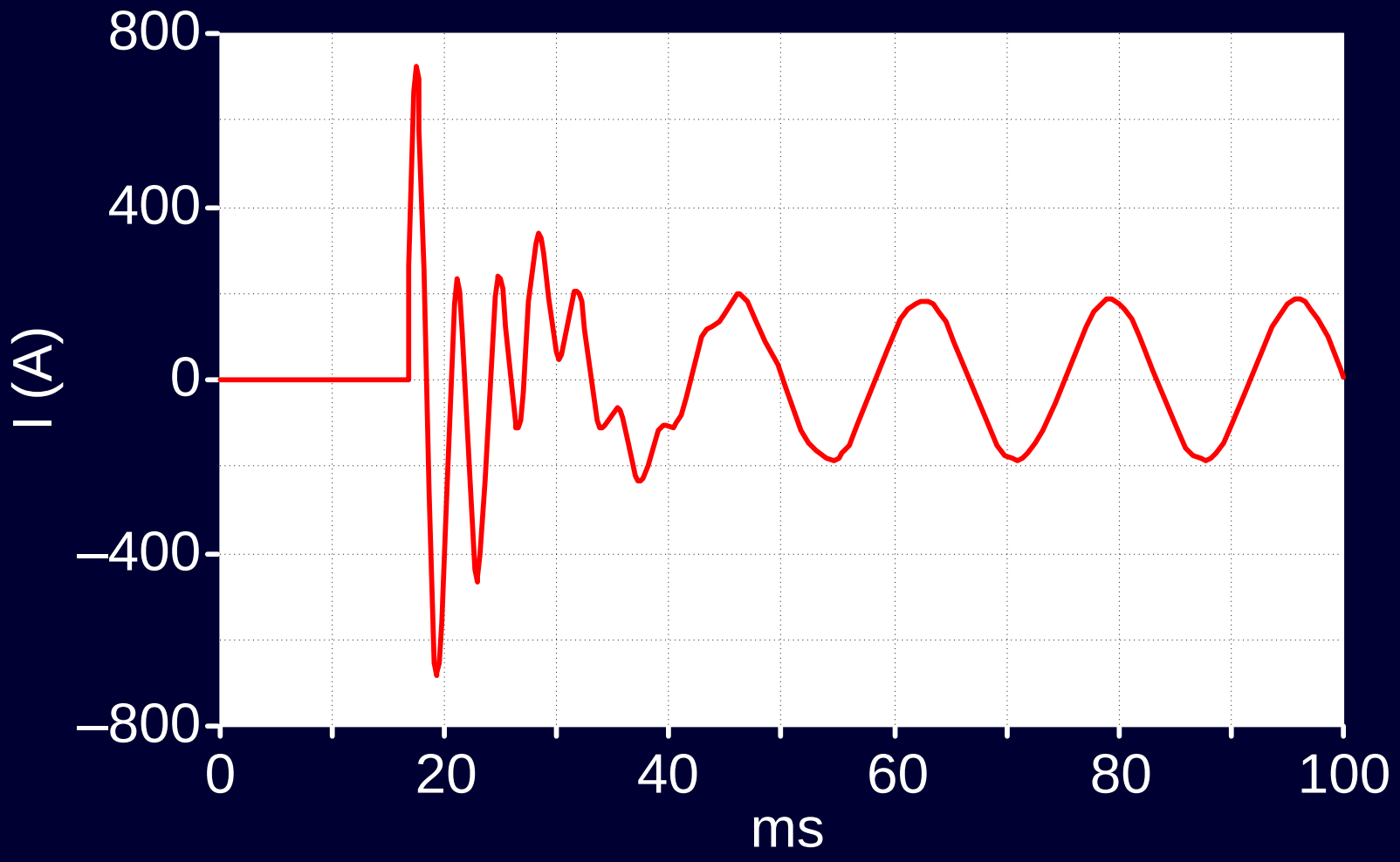
Characteristic impedance

$$Z_0 = \sqrt{\frac{L_S}{C}}$$

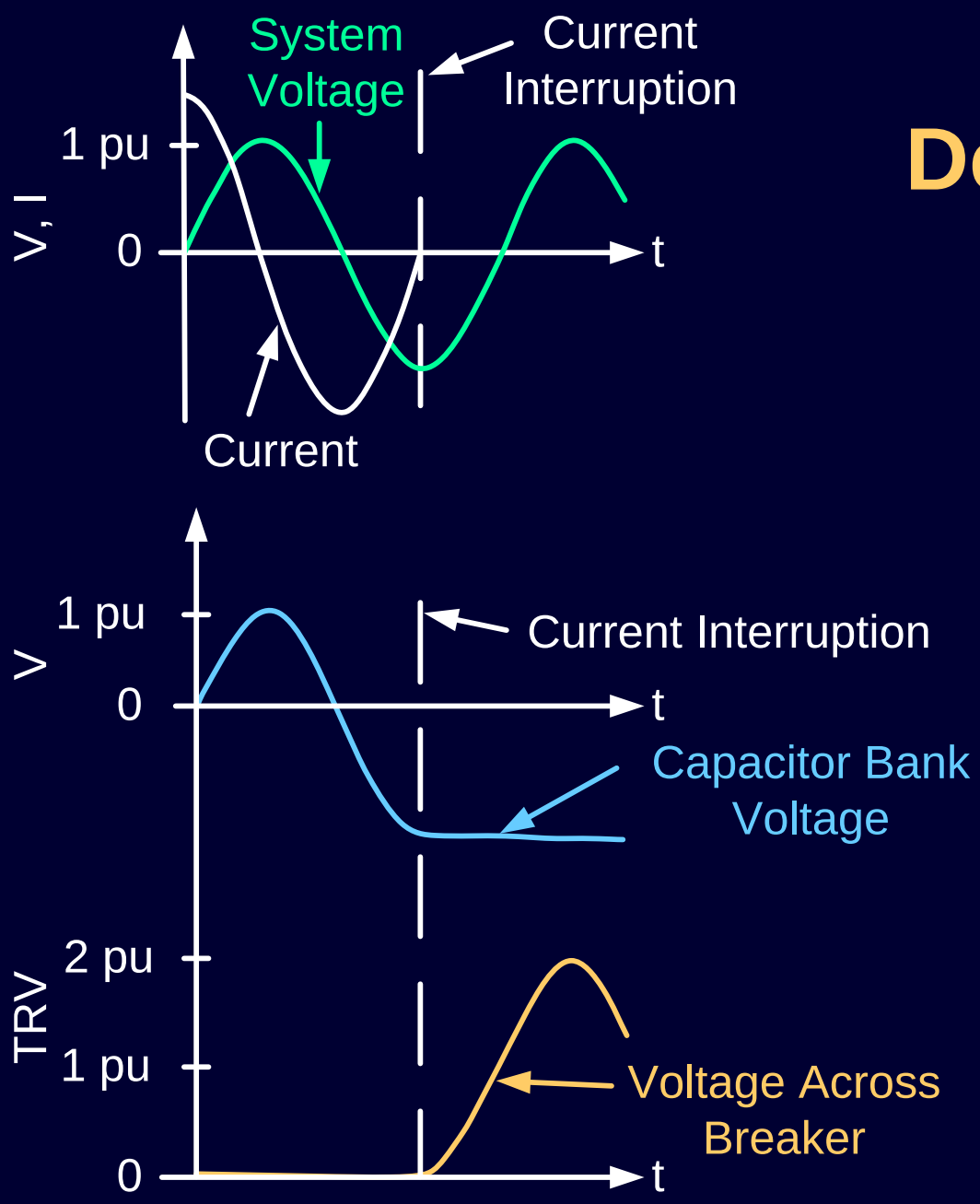
Resonant frequency

$$\omega_0 = \frac{1}{\sqrt{L_S C}}$$

Inrush Current



Capacitor De-Energization



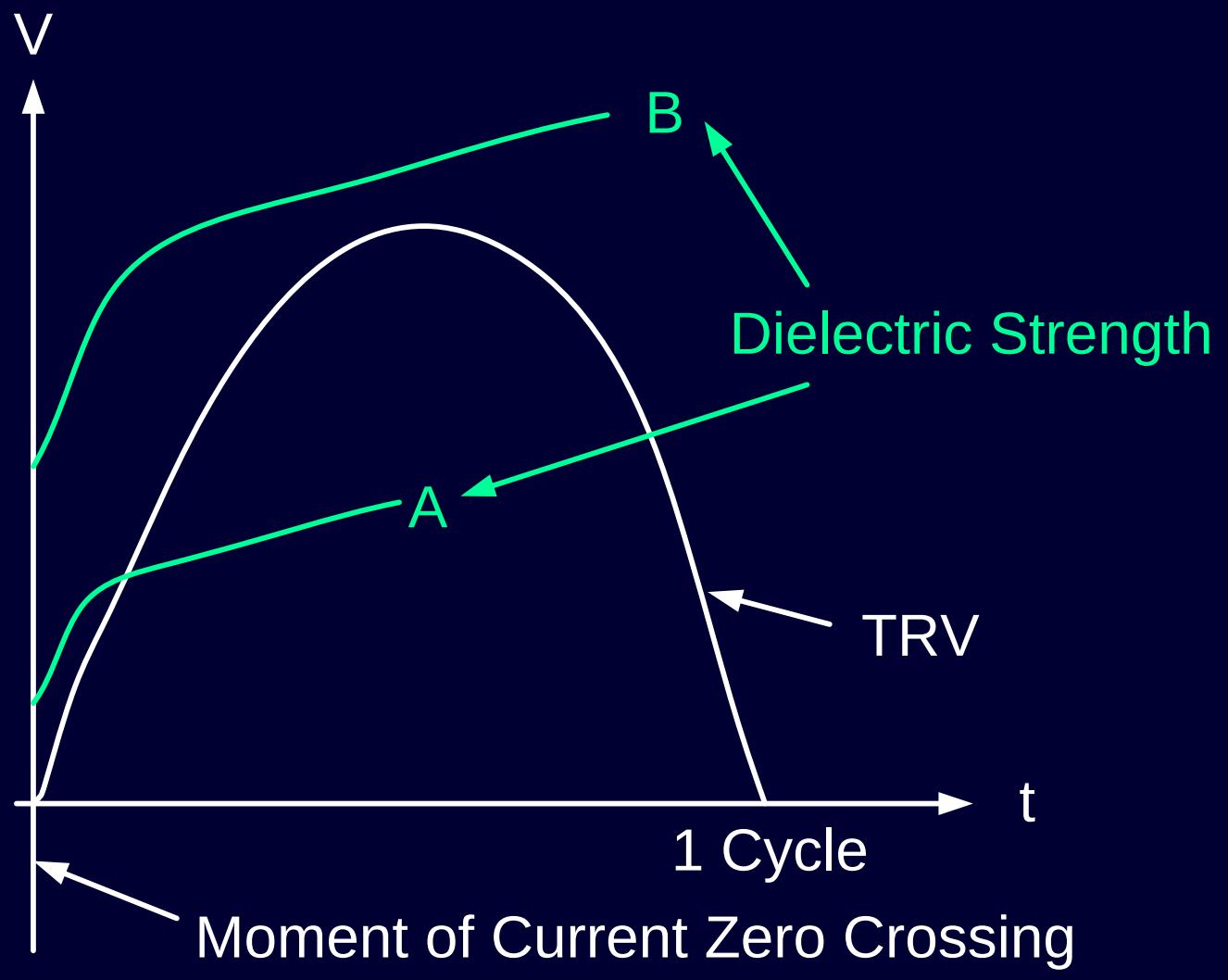
Transient Recovery Voltage

- Creates 2 pu voltage across circuit breaker
- May cause dielectric breakdown and reestablishment of current (i.e., restrike)

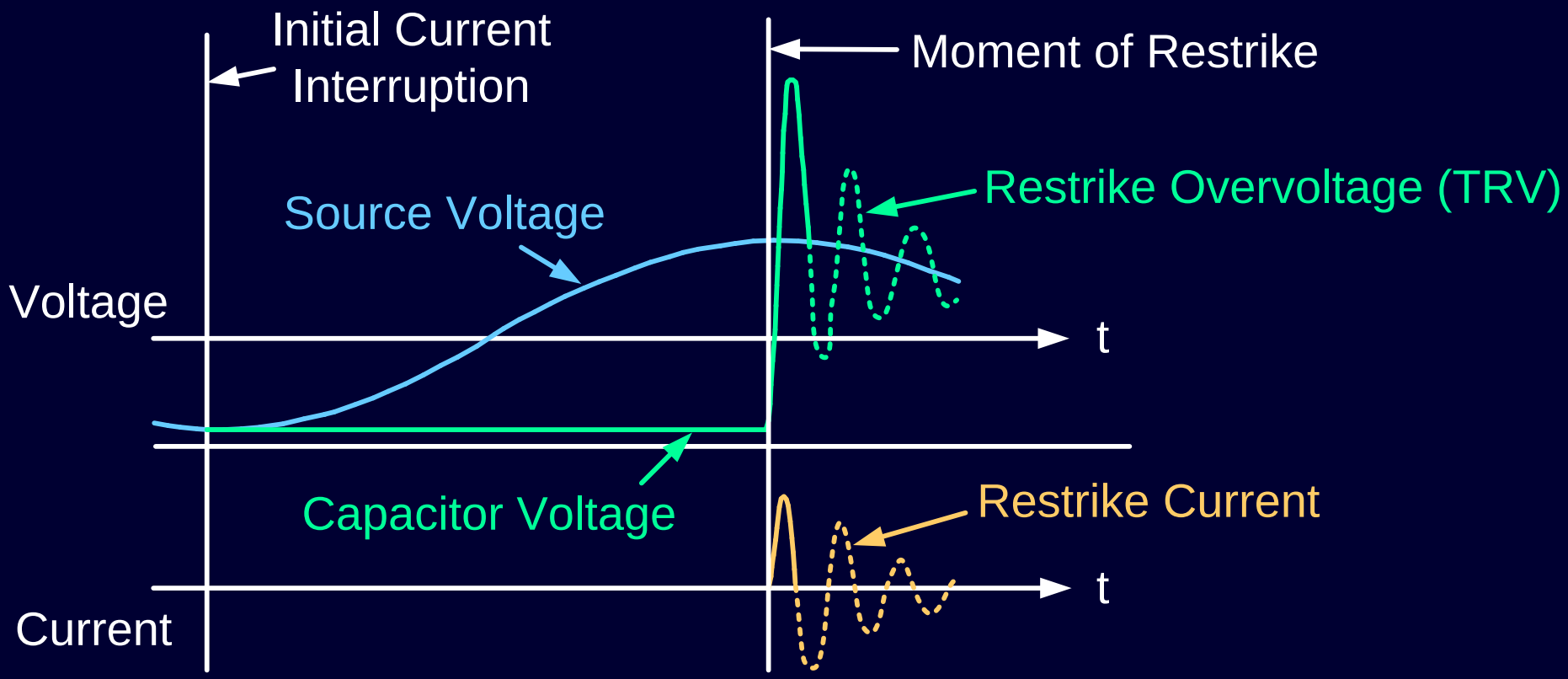
Circuit Breaker Opening

- Opening takes 2 to 5 cycles
- Dielectric strength increases as function of time
- Interruption effectiveness depends on where on current waveform breaker begins to open

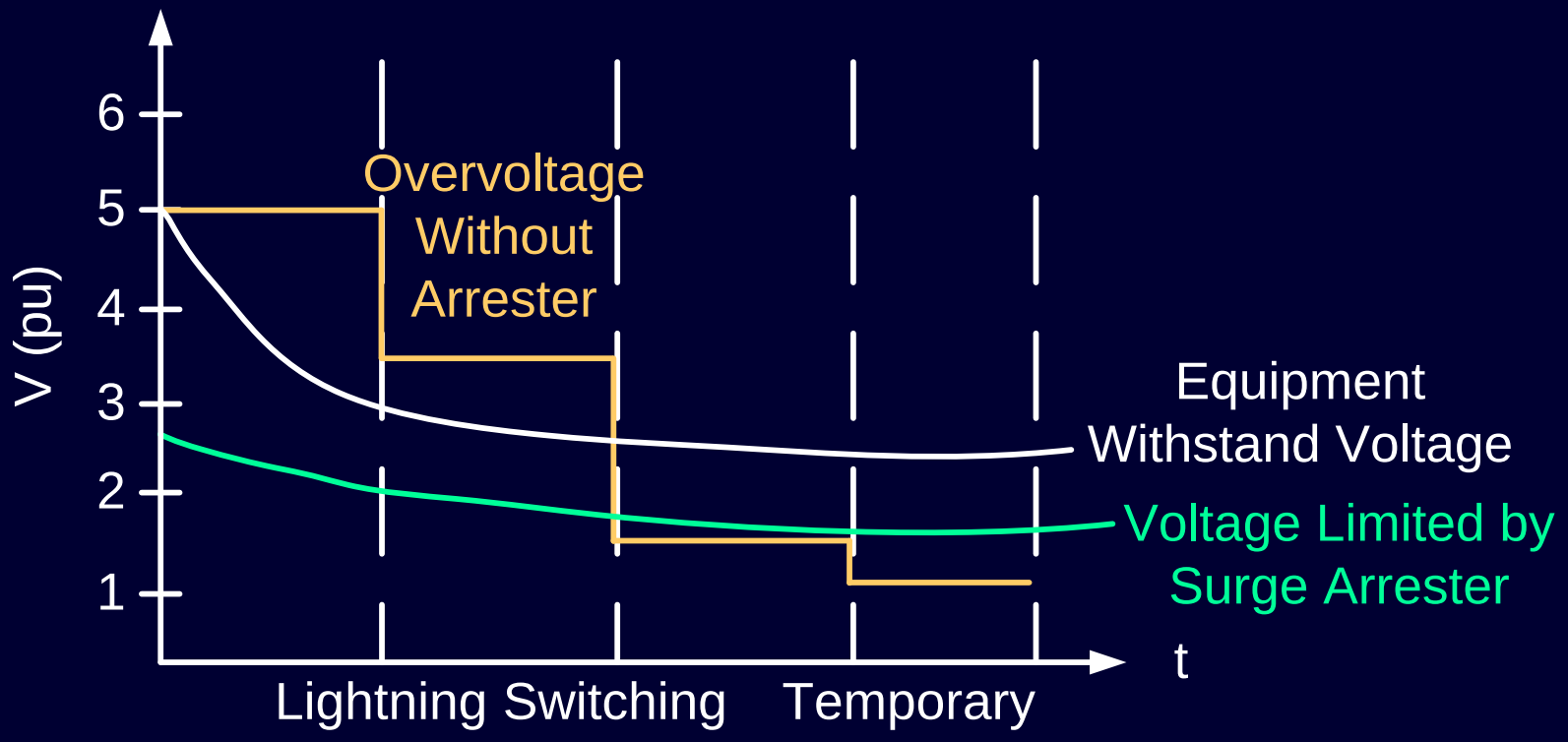
Dielectric Strength



Circuit Breaker Restrike Results in Severe Inrush Current That Causes Transient Overvoltage

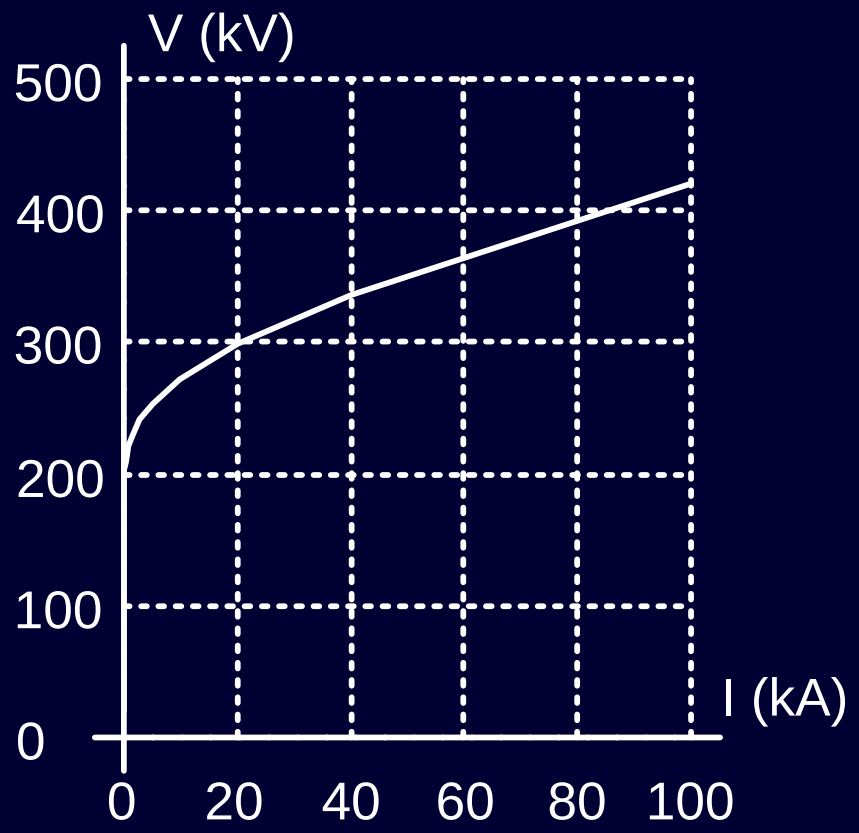


Protect Power System Equipment From Transient Overvoltages



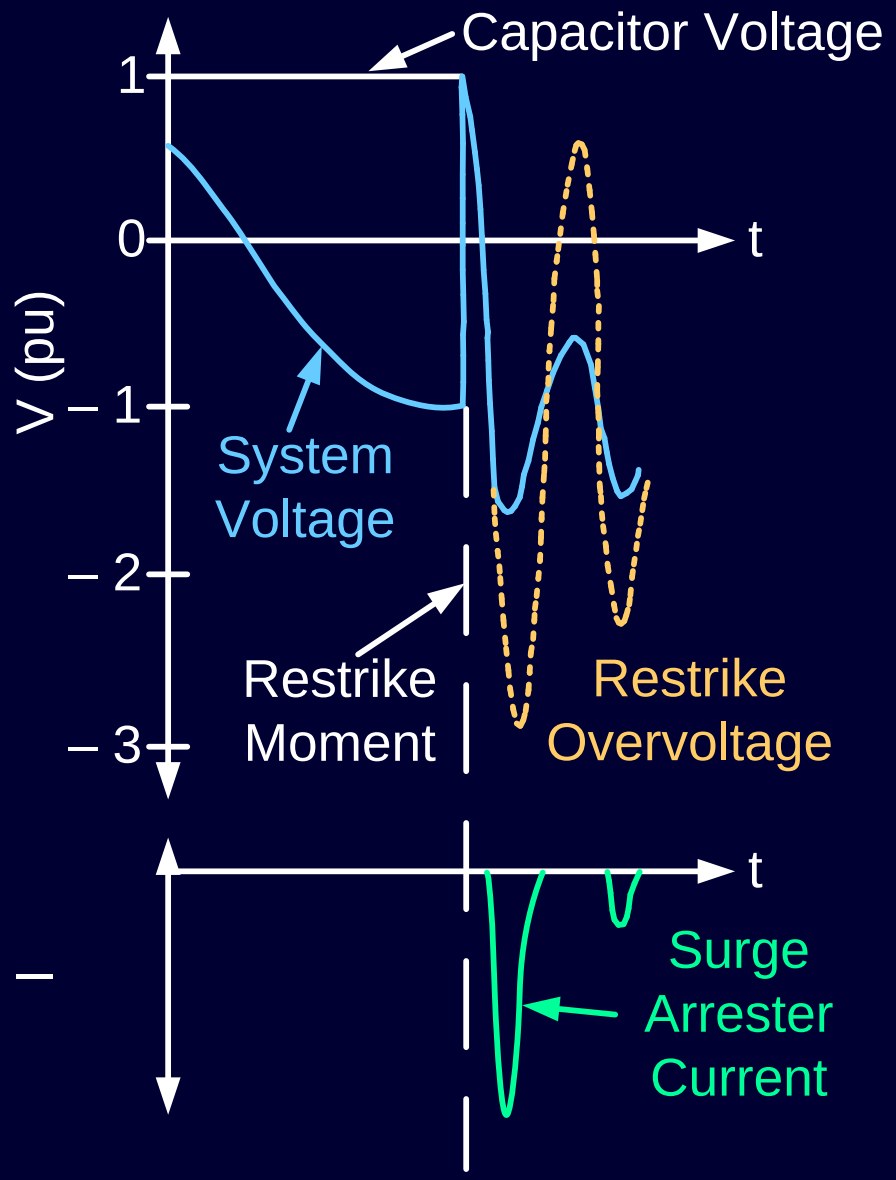
Surge Arrester Characteristics

- Metal oxide varistor (MOV)
- Extremely nonlinear V-I characteristics
- Thermal limits
  - Maximum operating voltage
  - Energy dissipation



Surge Arrester Current

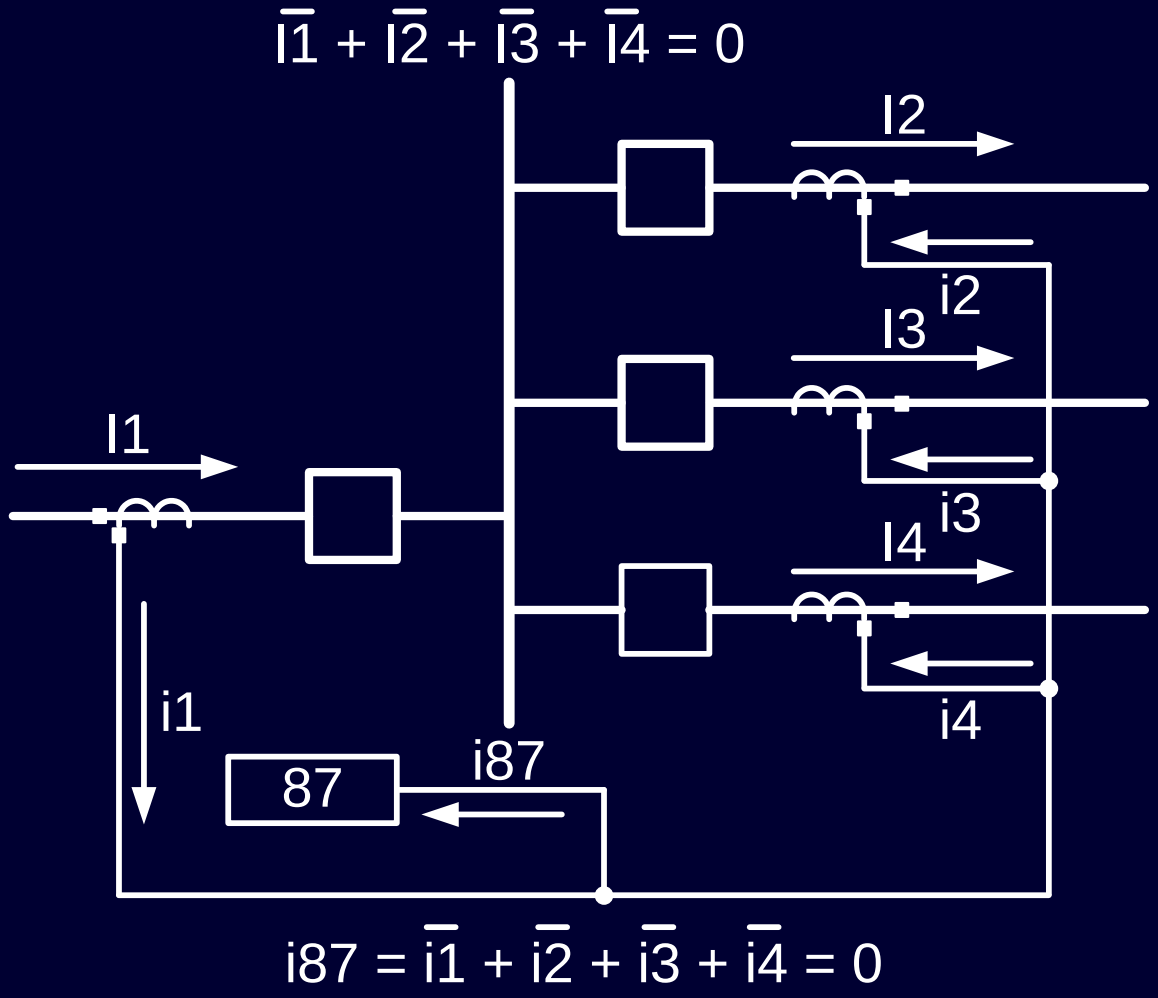
- Starts conducting at 1.75 pu voltage
- Conducts every other half-cycle



Bus Differential Protection

- Kirchhoff's current law says sum of currents entering and leaving bus or node must be zero
- Difference in currents indicates fault

Bus Differential Currents

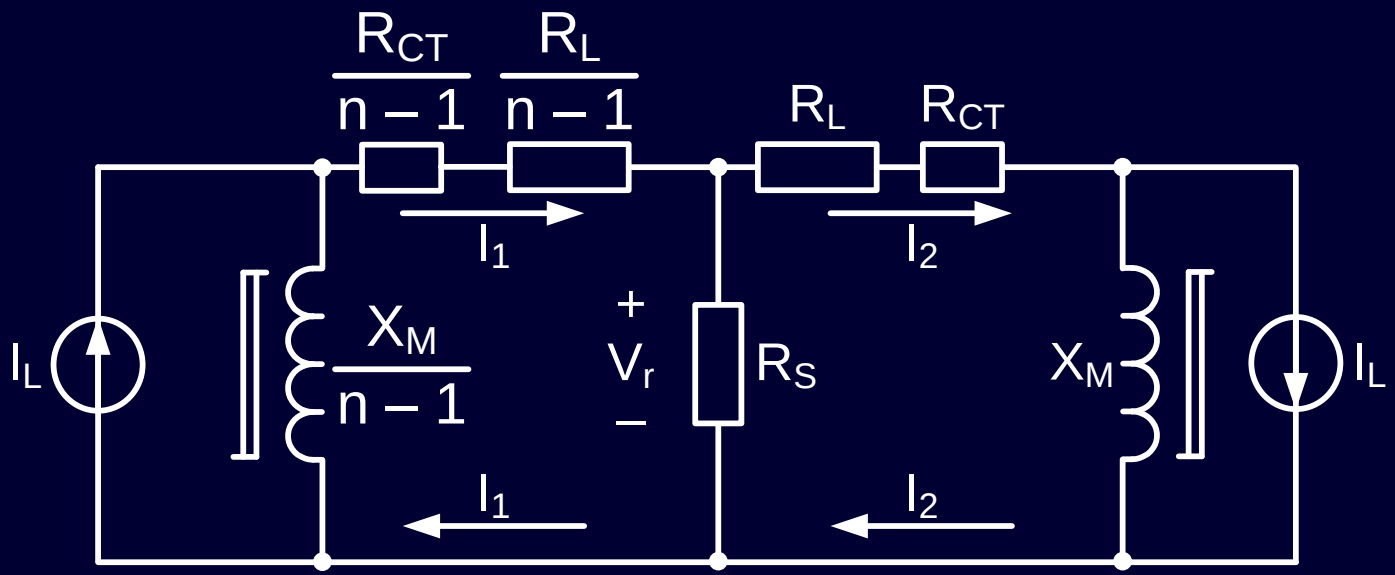


Current Transformers

- Conventional iron-core CTs may saturate regardless of ratio and accuracy class
- Saturation causes secondary currents to not represent primary currents

High-Impedance Bus Differential

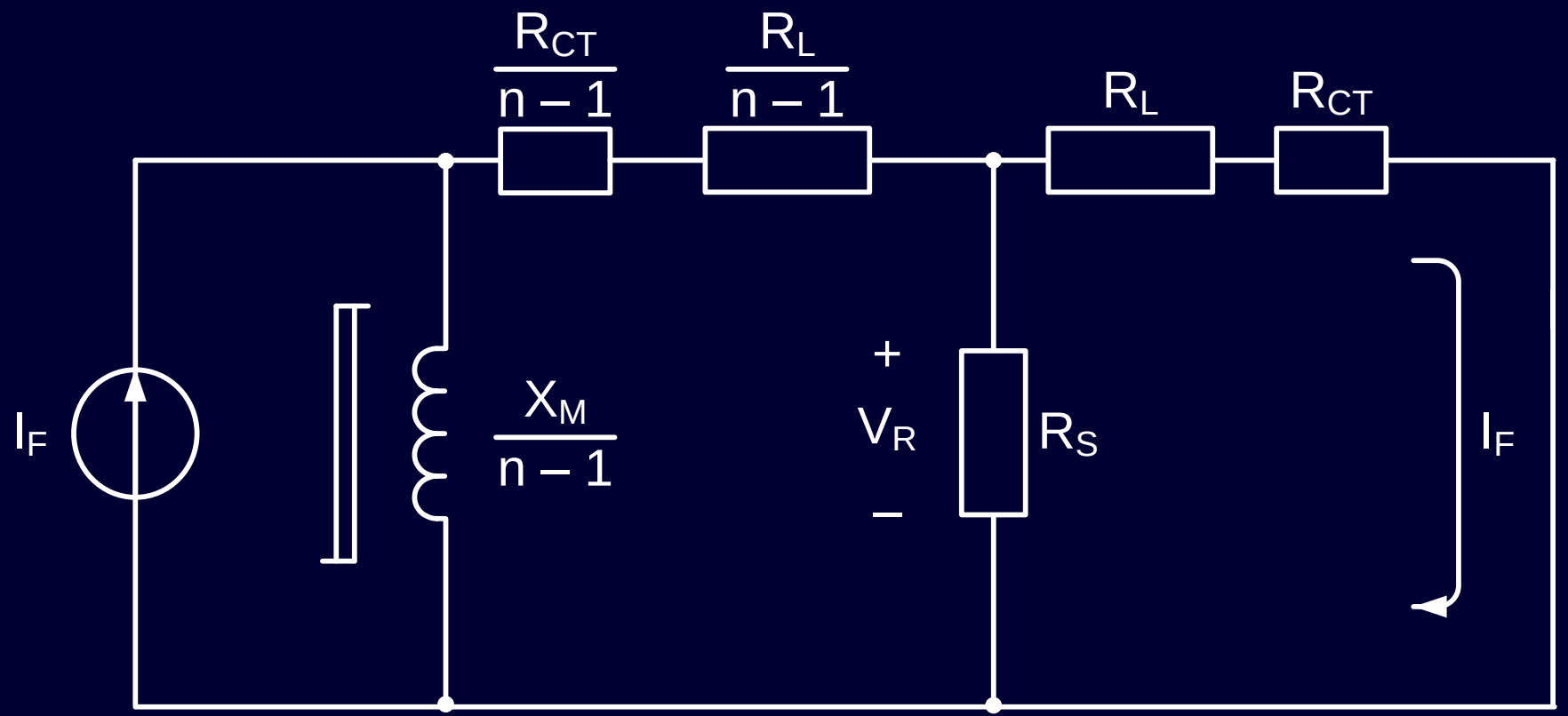
- During normal load and external fault conditions, secondary current circulates among CTs
- No current is flowing through relay



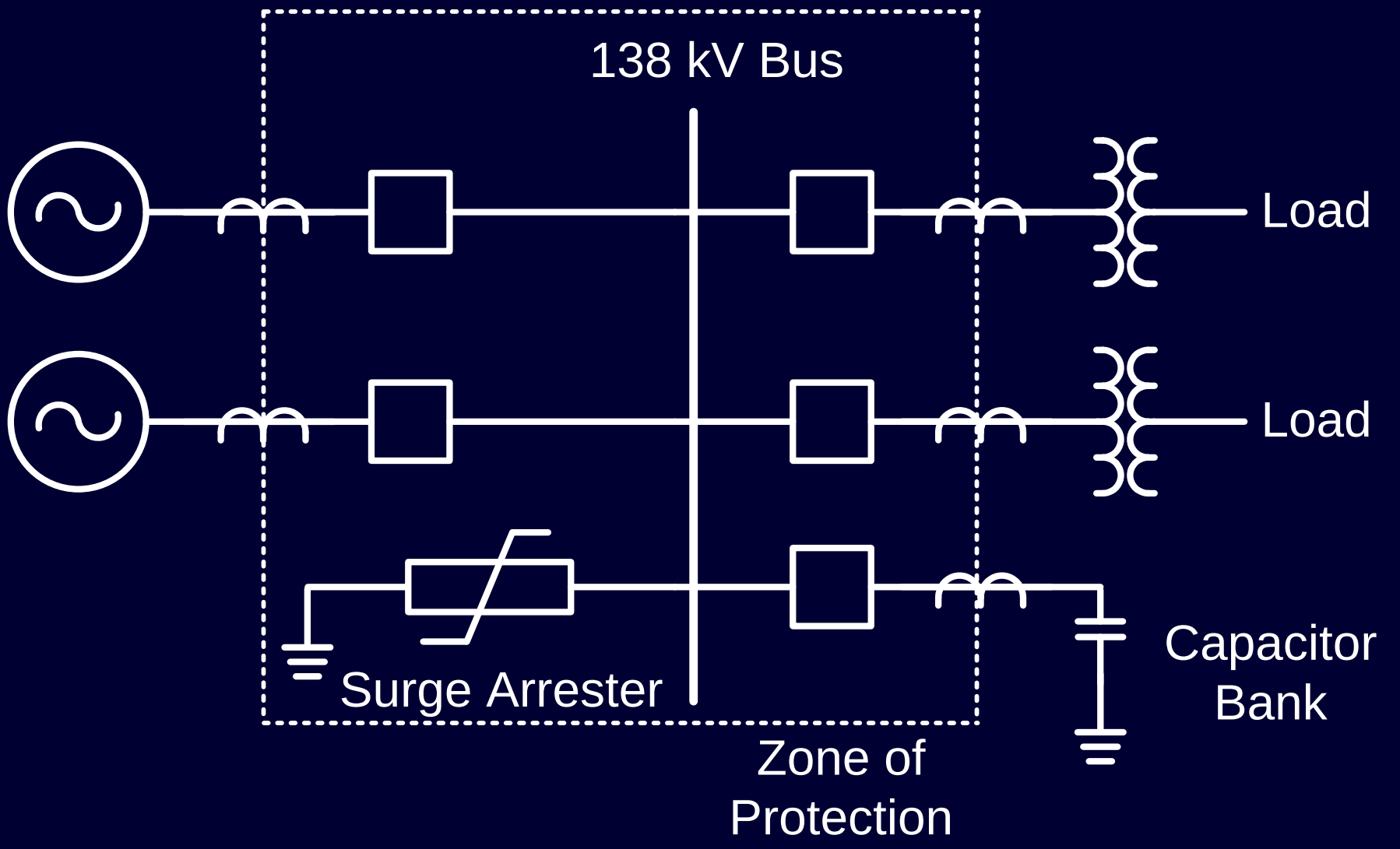
High-Impedance Bus Differential

External Fault With Faulted Feeder

CT Saturation



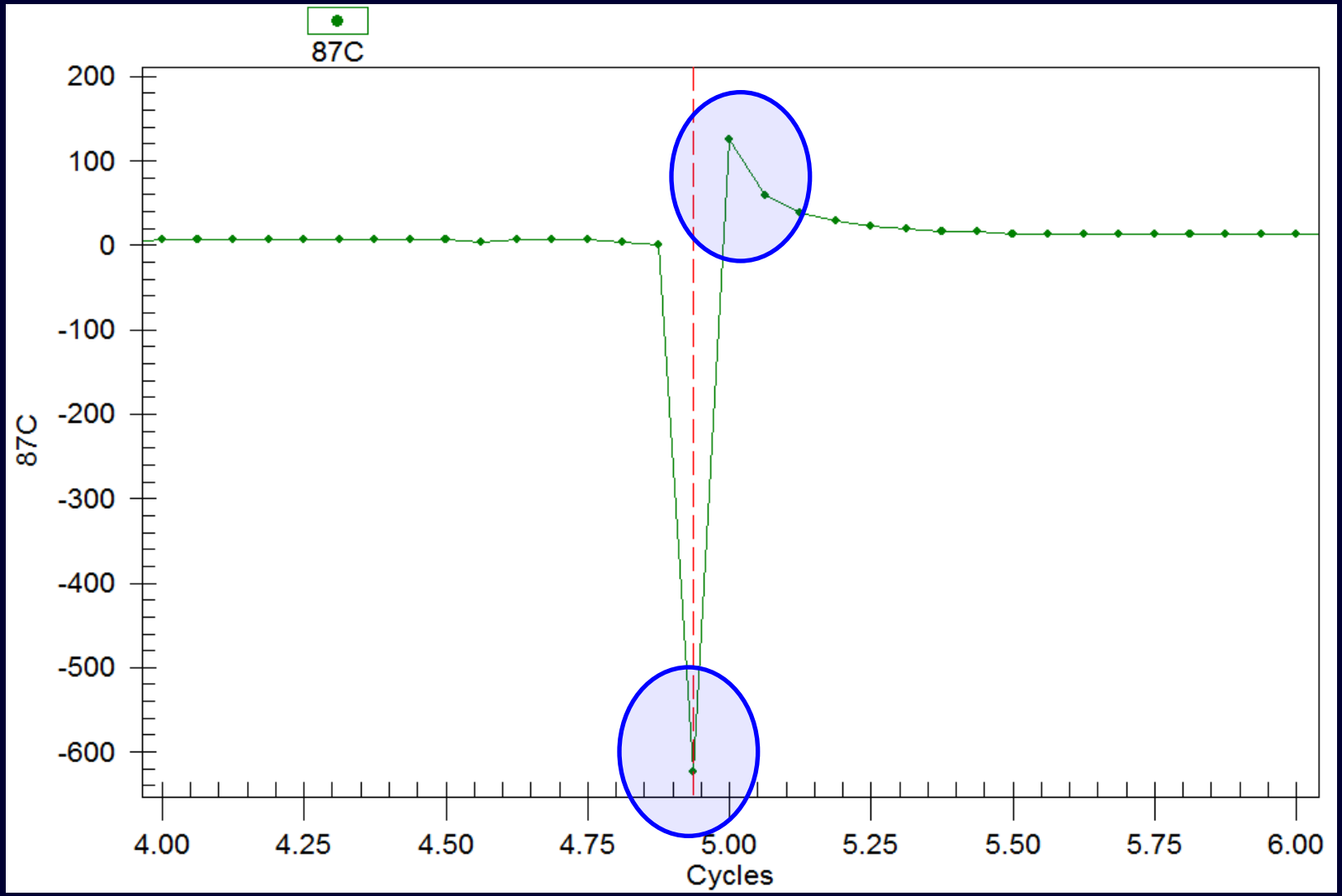
System One-Line Diagram



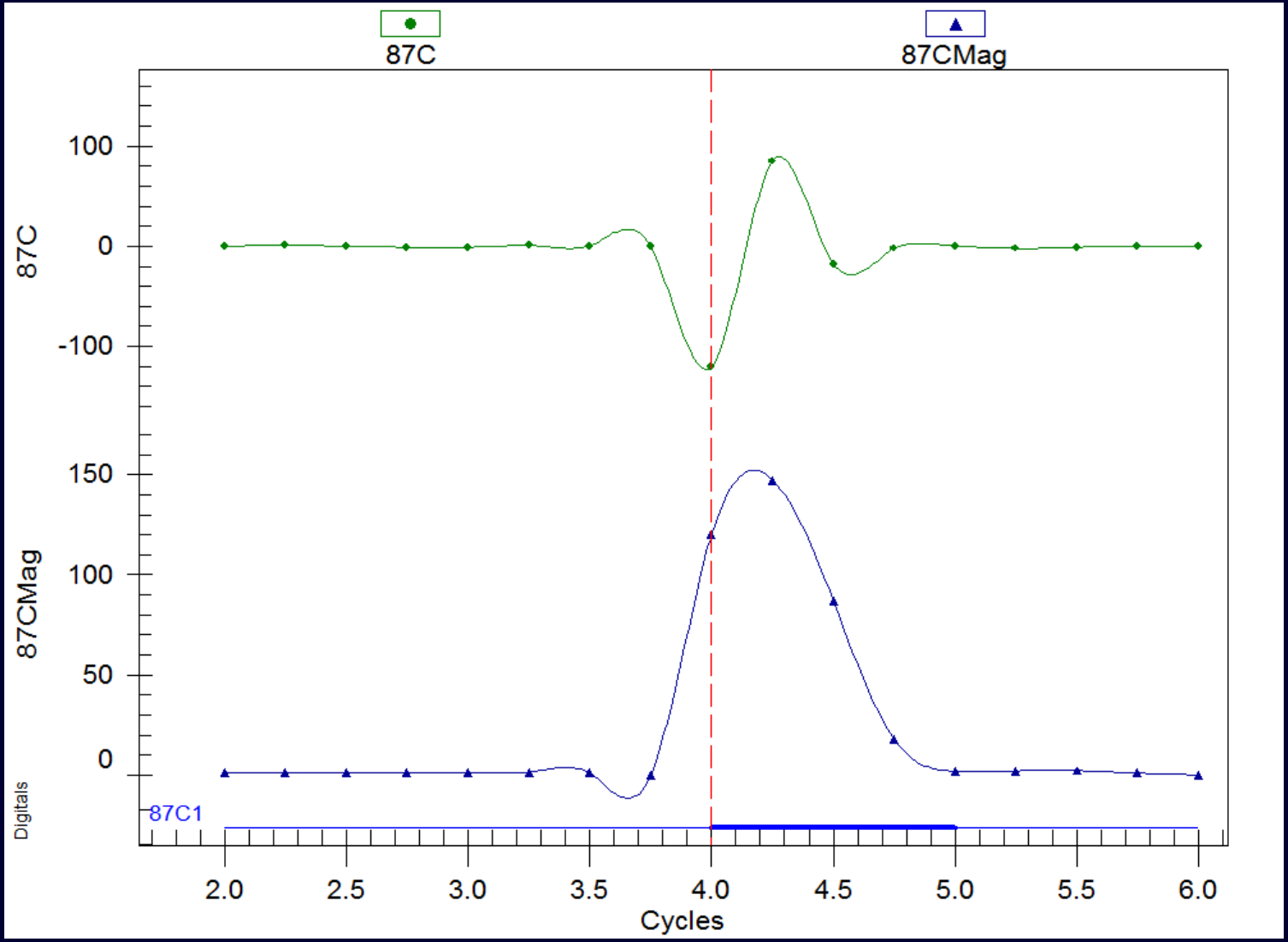
138 kV Substation

- 31.2 MVAR shunt capacitor bank
- 2000 A, 40 kA SF6 circuit breaker
- All CTs are C800
  - Feeder CTs are 1200:5
  - Capacitor bank CT is 2000:5 tapped down to 1200:5
- Surge arrester is station-class 84 kV MOV
- High-impedance bus differential set to 75 V

High-Impedance Bus Differential Raw Relay Event Report



High-Impedance Bus Differential Filtered Relay Event Report



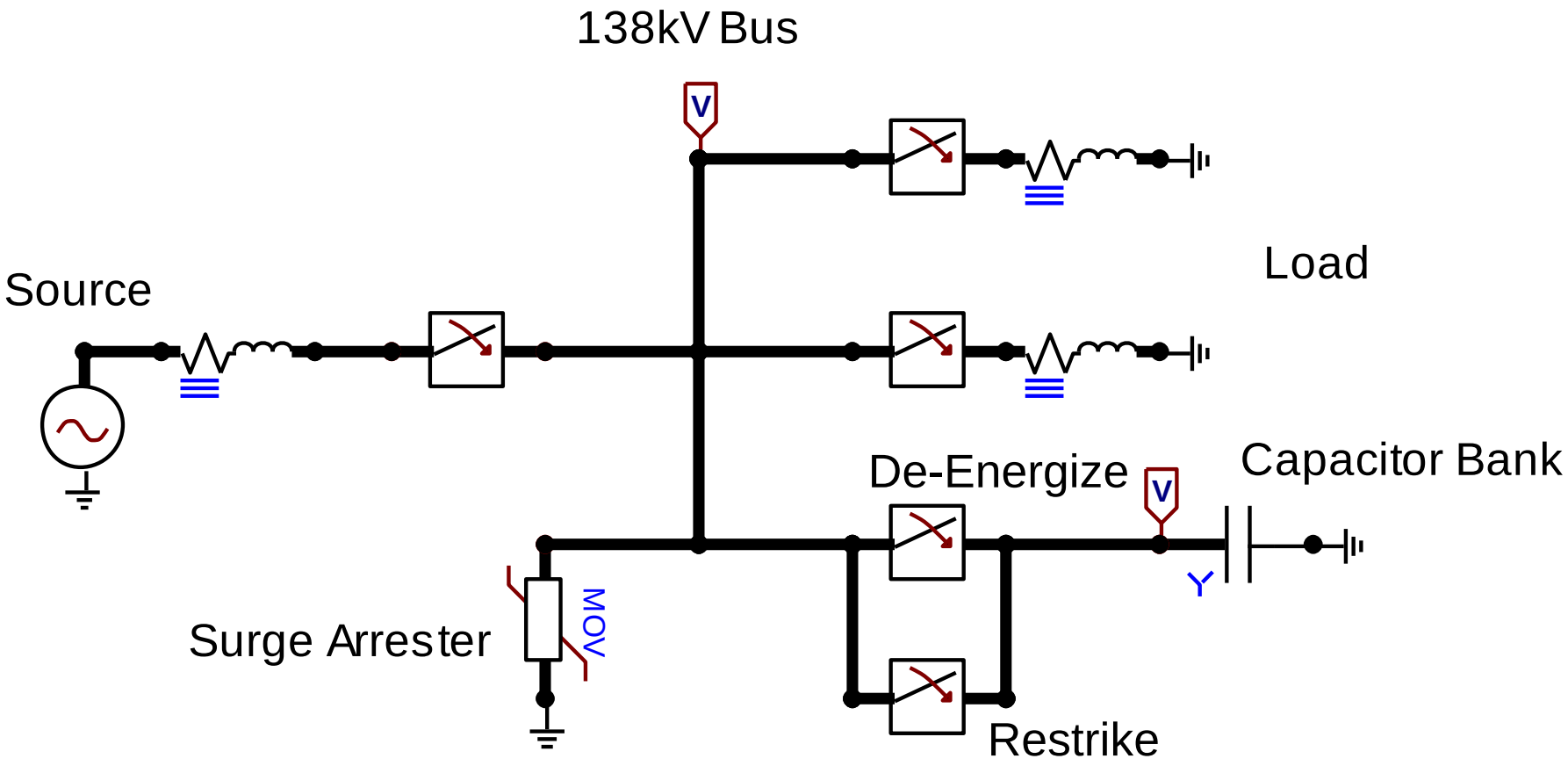
Proposed Theory

- Capacitor bank was de-energized
- Trapped charge maintained high voltage on capacitor
- Capacitor bank circuit breaker restrike created transient overvoltage at substation bus

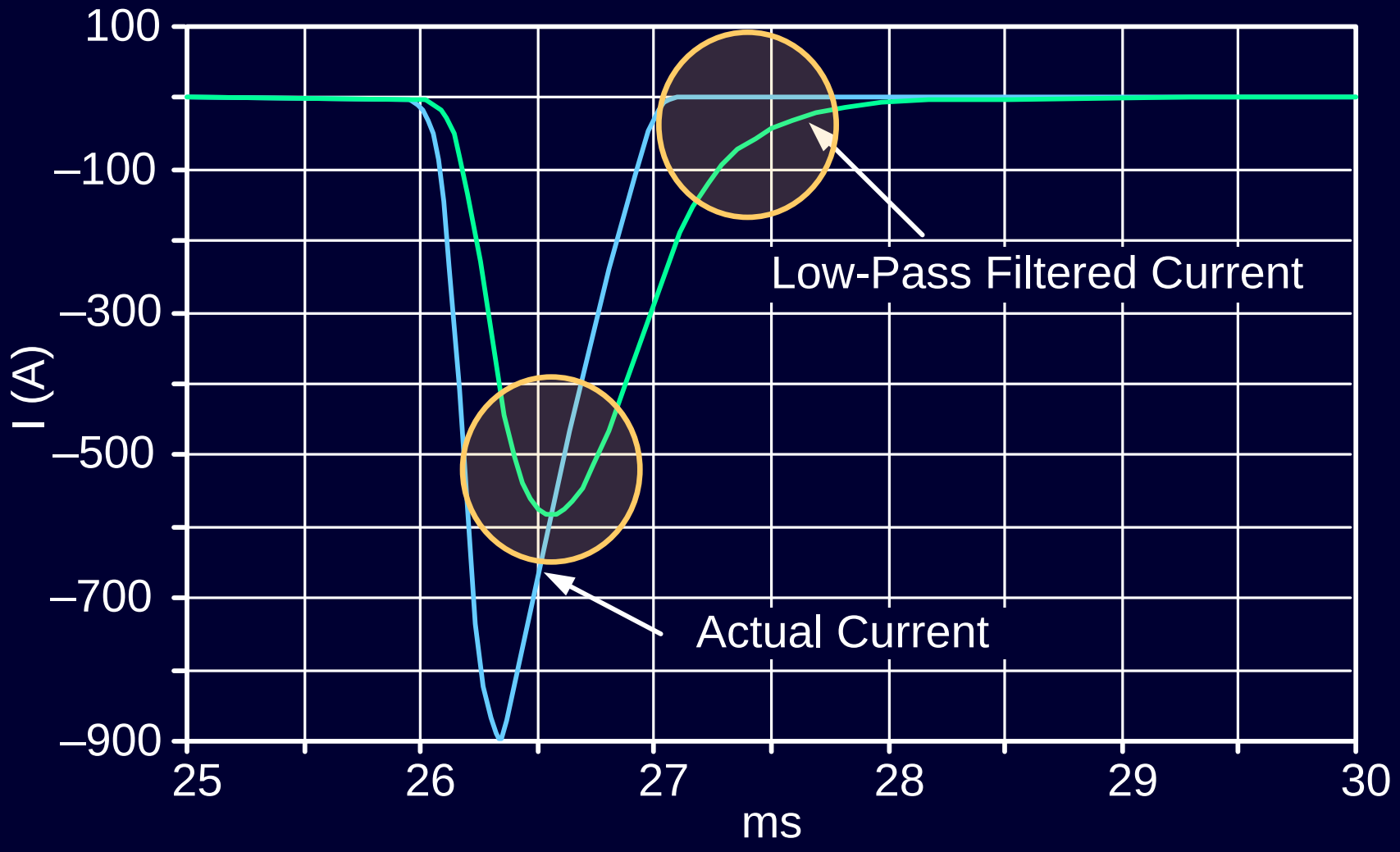
Proposed Theory

- Surge arrester located at bus started conducting current due to high transient overvoltage
- Surge arrester current appeared to high-impedance bus differential relay as differential current
- Relay tripped on differential current and de-energized bus

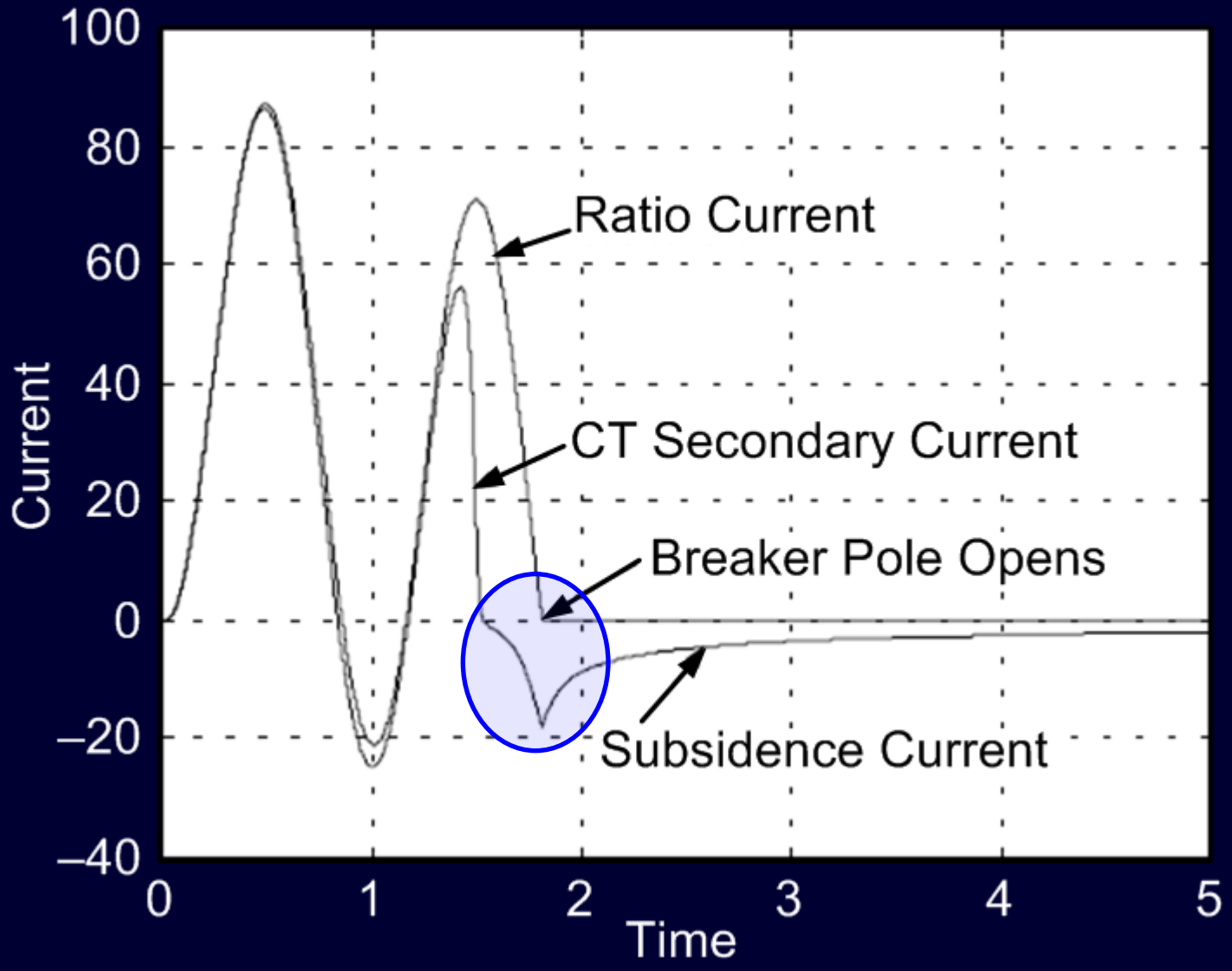
EMTP Modeling



Simulation Results

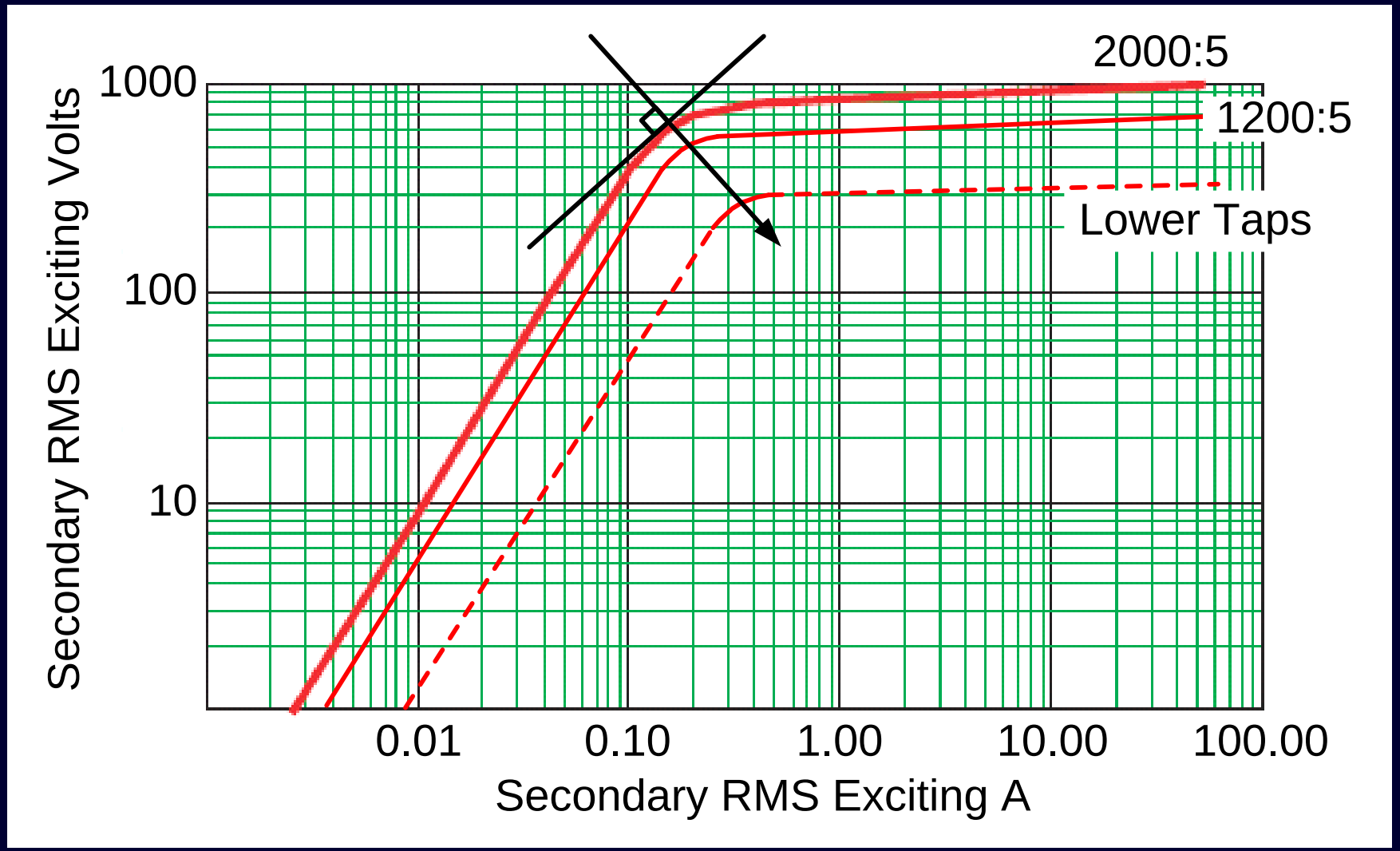


CT Subsidence Current

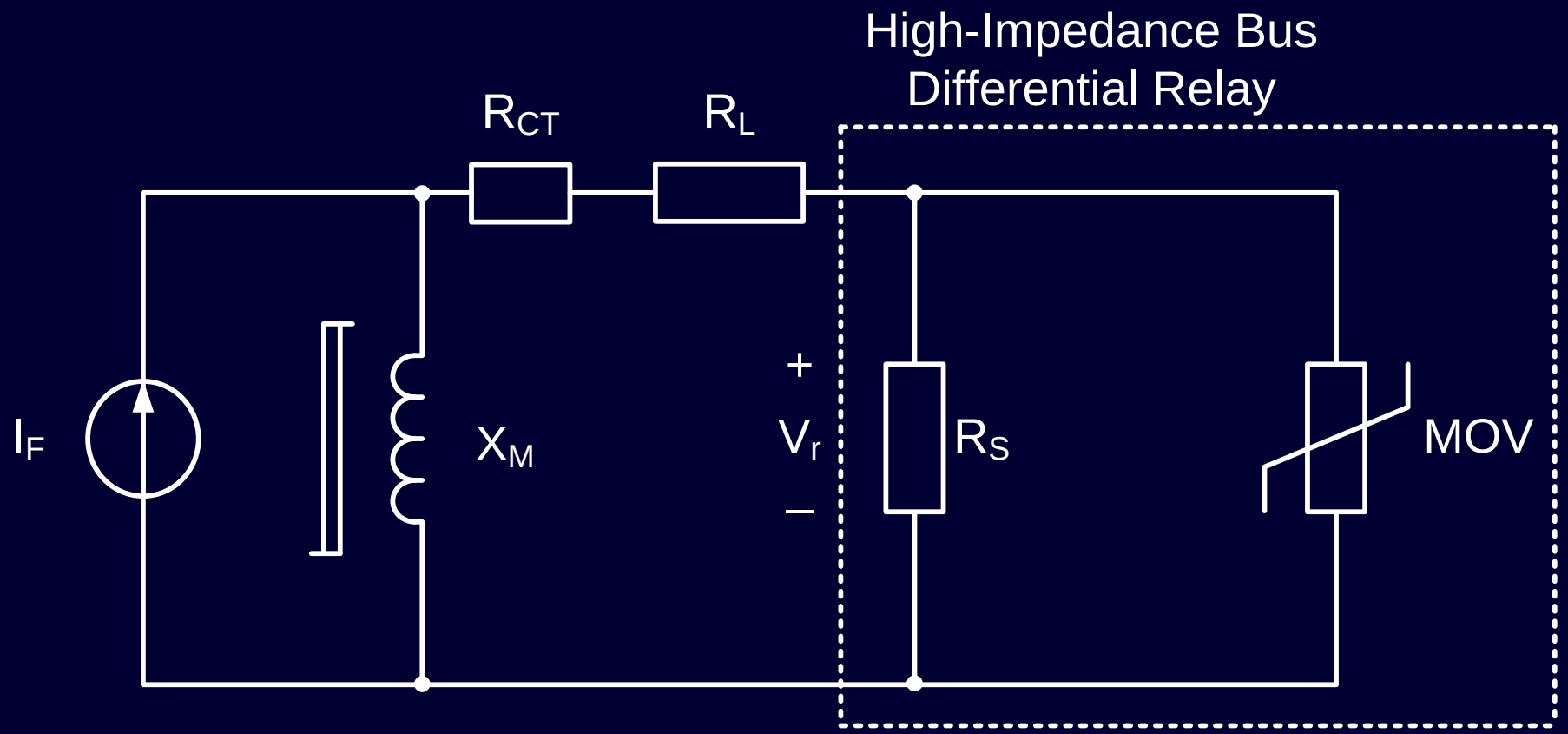


CT Saturation Curves

Tapped Down CTs Saturate at Lower Voltage



Voltage Across Relay

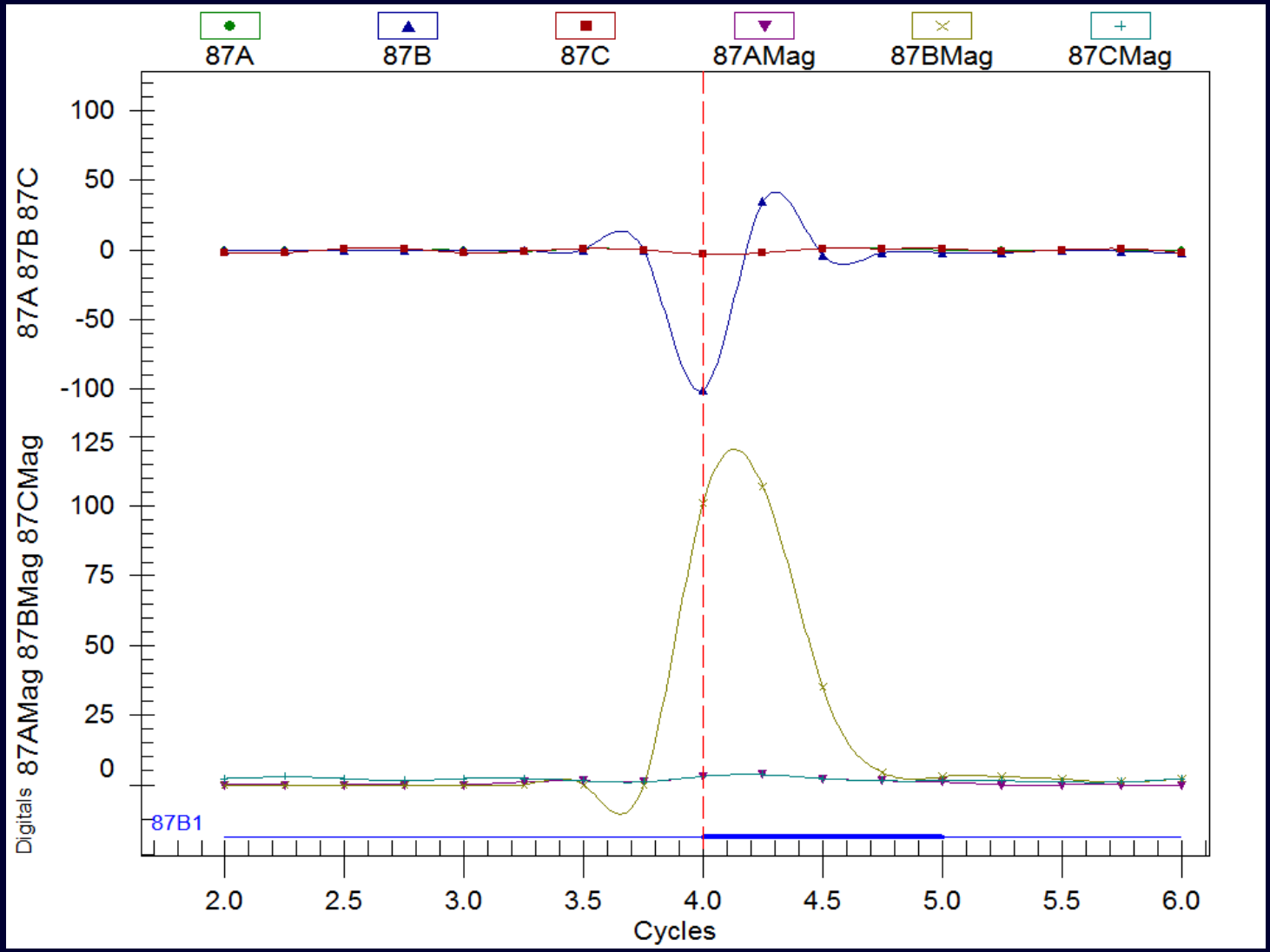


$$I_F = 240 \bullet \left[\left(4 \bullet 0.14 \bullet \sqrt{2}\right) + \left(1.0 \bullet \sqrt{2}\right) + \frac{600\ \text{V}}{2000\ \Omega} \right] \text{A}$$

$$I_F = 600\ \text{A}$$

Review of Event Data

Previous Case Three Years Prior



Settings Recommendations

- If surge arrester is within zone of protection, add at least 1.5-cycle time delay
  - 0.5-cycle event (increasing voltage setting may reduce)
  - 0.75-cycle filter delay
  - 0.25-cycle safety margin
- Too long of a time delay can decrease protection dependability, especially when lower-class CTs are used

Conclusion

- Capacitor banks on power system
- Transients due to capacitive switching
- Surge arrester operation
- High-impedance bus differential protection
- Real-world event analysis showing relay misoperation due to circuit breaker restrike
- Settings recommendations

Questions?